Hardware Project for CMPE310

Assigned: Tuesday, April 02
Due: Tuesday, April 09 (midnight)

Project Description: Design a simple memory system in Concept-HDL.
The design consists of two memory chips, a PROM and a SRAM, both 2Kx8 devices. You can use any other devices, i.e. decoders and gates, as required for the libraries given.

The system specifications are given below:

Parameter	Specification
Project Name	310_Proj4
Libraries to be included	a74lsttl, memory
Design Name	project4
PROM chip	CY7C291 2kx8
PROM address range	[00]000H - [00]7FFH
SRAM chip	CY7C128 2kx8
SRAM address range	[00]800H - [00]FFFH
SRAM parameters to be set	Size = 8

The following is the list of input/output ports of you design. Use the same name, size and direction as mentioned below. You can use any other names for internal wires.

Signal Name	Direction	Size (bits)
address	IN	8
data	IO	14
read	IN	1
write	IN	1

The testbench to be included for the project is called *project4_test.v,* the link to which is given with this description. Change the following line to reflect you design (as discussed in class).

defparam instance1.page1_i1.MEMORYFILE = ("./project4_input.dat");

The link to the data file *project4_input.dat* is provided with this description. Copy the data file and change the path in the above line to reflect it. Also change the instance hierarchy to match your design. **Copy both the *project4_test.v* and *project4_input.dat* in the project directory.**

Tar your project directory using *tar -cvf project4.tar <your_directory_name>*.
Gzip it using the command *gzip project4.tar.*
Submit the *project4.tar.gz* file.

ANY FORM OF CHEATING WILL RESULT IN A ZERO FOR THE PROJECT AND THE APPROPRIATE DISCIPLINARY ACTION AS MANDATED BY UNIVERSITY POLICY.