LAB Assignment #3 for ECE 337

Assigned: Wed., Oct. 26, 2011
Due: Wed., Nov. 2, 2011

Description: Write the VHDL code that implements a shift register.

In your current design, you have two registers, A_op_reg and B_op_reg, that are loaded with the binary representation of two values that you enter using putty. In the previous lab, pressing BTN1 simply added the binary values, converted the result to ASCII and wrote the ASCII result to the serial port.

In this assignment, you will enter 2 values (as you did above), but will have the option of pressing BTN2 before pressing BTN1. When you press BTN2, your VHDL module should read the 12-bits of B_op_reg, one at a time, and shift them into a new shift register (created within your module) i**n reverse order**. For example, if you enter the value 8, it's binary representation is 000000001000. After pressing BTN2, the shift register should contain 000100000000 (which represents 256). Also, if BTN2 is pressed, you should remember this by also creating a 1-bit FF in your module that is set to 1 when the user presses BTN2. This 1-bit register should to be reset to '0' when reset is pressed (NOTE: reset is already connected to BTN0 on your board). The output of this 1-bit FF should drive the select input to a 2-to-1 MUX that I have inserted into the new version of the UARTNumberConvert.vhd file. The 2-to-1 MUX is setup to add A_op_reg with either B_op_reg or B_op_reverse_reg, i.e., the output of the shift register you created in your VHDL module.

In summary, once you enter 2 values using putty, if you press BTN1, then you simply output the sum of the two values. This is exactly what happened in lab2. If, on the other hand, you press BTN2 before pressing BTN1, then the sum is computed using A_op_reg and the reverse binary value of B_op_reg.

I created new signals 'but2_pressed', 'B_op_reverse_reg' and 'B_op_outputs' as well as the 2-to-1 MUX in the UARTNumberConvert.vhd file (available on my website under lab3_files). You need to create a VHDL module that implements the entity instantiation given in UARTNumberConvert.vhd file (shown below).

```
ShiftBOp: entity work.ShiftBOp(beh)
   port map (clk=>clk, reset=>reset, B_op_reg=>B_op_reg,
      B_op_reverse_reg=>B_op_reverse_reg,
      but2_pb_stable=>but2_pb_stable,
      but2_pressed=>but2_pressed);
```

Laboratory Requirements:

1) In class DEMO on the due date.

Grading:
100 pts will be given for a proper demonstration.