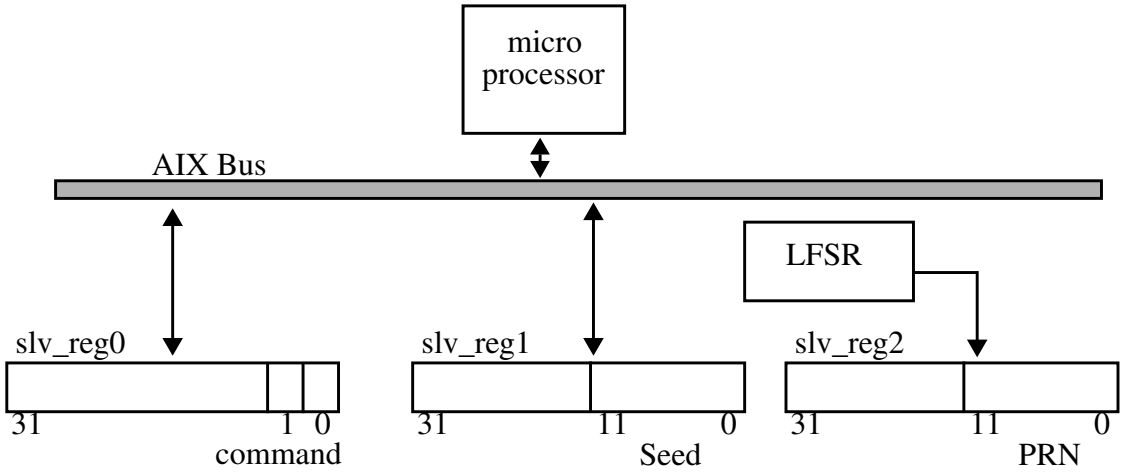
LAB Assignment #1 for Hardware/Software Codesign with FPGAs

Assigned: Mon., Sept 23, 2013
Due: Mon., Sept 30, 2013

Description: Implement a slave peripherial and incorporate an LFSR.

Implement your slave peripherial with 3 registers following the process described in class. The overall simple architecture is given in the figure below.



"00": Preserve contents
"10": Load seed
"01": Shift LFSR, 1 bit per clk

You need to change the USER_LOGIC.vhd to include the LFSR.vhd file (provided on my web-site). You also need to create a C program that implements the following pseudo-code:

```
read/print slv_reg2 ->1
write seed slv_reg1 1023
write slv_reg0 2
read/print slv_reg2 ->1023
write slv_reg0 1
write slv_reg0 0
read/print slv_reg2 -> 694 or 1388
```

The values after '->' should be the output from your C program printed to a serial-port-connected terminal window running on your laptop.

SDK: right click src folder in tree hierarchy -> C/C++ general -> Paths and symbols
Add 2 include paths:
1 for peripheral header file:
(C:\Users\BCubest_LFSR_periest_LFSR_peri.srcs\sources_1…dkroc_module†riversıfsr_peri_v1_00_a\src)
1 for xbasic_types.h directory:
(C:\Xilinx\14.6\ISE_DS\EDK\sw\XilinxProcessorIPLib†rivers\common_v1_00_a\src)

Prepare to demo this in class.