LAB Assignment #0, Part 6, for ECE 522

Description: Create the design_1_wrapper.vhd file and a Screen Snapshot of Vivado after you have successfully synthesized the GPIO BRAM project

In this sixth lab, you need to create the design_1_wrapper.vhd file and add it to the project as described in the VivadoPLAndBlockDiagram video. Once you have removed all syntax errors and have successfully added it to the project, upload the design_1_wrapper.vhd file directly (do NOT insert the text into a PDF).

Also, create a screen snapshot of Vivado after you have successfully synthesized the GPIO BRAM project from the VivadoPLAndBlockDiagram video, as shown below, insert the image into a document and upload as a PDF. This will allow me to confirm that you have successfully created the design_1_wrapper and synthesized the project.