Verification of Convolution Relation Between Sensitized Path's Gate Transients, Power Grid Impulse Responses and Power Port Transients

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Abstract

In this paper we provide further evidence and verify the existence of convolution relation between transient currents of gates of a sensitized path, power grid impulse responses and transient currents measured from chip power ports. Such a relation has important implications and applications in different aspects of current based testing and diagnosis techniques. We have also developed a new tool for extraction of sensitized path's circuit model from chips SPICE model. Our simulation results shows that using the new flow for path extraction will improve the accuracy and generates waveforms that are closer to full chip SPICE simulation.

1. Introduction

Current based testing and diagnosis techniques can be broadly partitioned into two groups; those based on I_{DDQ} and those based on I_{DDT}. I_{DDQ} methods, e.g., [1] through [7], have been very effective in the past for detecting and locating shorting defects but are increasingly less effective given the leakage current trends in newer process technologies. In addition to the problem of growing leakage currents that makes I_{DDQ} methods less effective, I_{DDQ} test and diagnosis suffers from other deficiencies like the inability to detect and diagnose delay defects, such as resistive open defects.

As an alternative approach chip's transient power supply signals, I_{DDT}, can be measured and analyzed. Despite the challenges in accurate measurement of I_{DDT} waveforms from chip power supplies, that has so far been a main obstacle in wide spread application of these techniques in industry, I_{DDT} techniques have a number of favorable properties that can make their use very fruitful and interesting. I_{DDT} based methods are generally robust to increases in leakage current and can be applied to virtually any type of logic, including dynamic logic. Moreover, due to the fact that measured transient waveforms contain interesting timing and power consumption information, signal processing methods can be employed to extract such important information. For example I_{DDT} techniques have the potential to detect and locate defects that affect delay, such as resistive opens. Several I_{DDT}-based diagnostic techniques have been proposed in the literature.

A fault localization method is proposed in [8] that analyzes the area under I_{DD} waveforms as a means of extracting delay information. This delay information is used to estimate the "logic depth" at which the fault occurs. In [9], a fault localization technique is proposed that is based on the charge delivered to the chip during a transition. A wavelet transform analysis of the power supply transient signals is proposed in [10]. Defect localization is achieved by mapping the time at which the wavelet transform coefficient of the defective chip differs from that of the defect-free chip into logic depth.

A fault simulation engine based on fast simulation of chip's power port I_{DDT} signals was developed in [11]. The main idea behind the fast simulation of transients was that the power grid structure of chip can be considered as a linear system where the inputs are the individual gate transients and the outputs are observed power port transients. Therefore, there must be a convolution relationship between the transients of each of the gates of the sensitized paths, the impulse responses of the power grid and the transients observed at chip power ports. Hence, to speed up the calculation of power port transients, rather than performing full chip SPICE level simulations one can extract the sensitized path, perform the simulation only on that path, and also characterize the chip power grip and obtain the impulse responses via simulations. Then via convolution of the gate transients obtained from path simulation to the grid impulse responses, one can obtain the chip power port transients. This process will be significantly faster than full chip simulation because an individual path is much smaller than the whole chip and power grid characterization and calculation of its impulse responses is a one time process for each chip and can be done independent of a specific path. In [11], simulation on a benchmark circuit where employed to demonstrate that the outcome of calculating power port transients through convolution, is close to full chip accurate SPICE simulations. However, there were some notable levels error between the SPICE simulation results and convolution process outputs.

Existence of convolution relation between gate transients, grid impulse responses and observable power port transients, if further proven to be correct, has very important and interesting implications because it directly relates the measurable transients (I_{DDT}) to the transient of the gates in the chip that are not accessible or measurable. Hence, one can measure the power port transients and by reversing the process (i.e. deconvolution) obtain insight about the status of each individual gate in the chip.

In [12] we developed a defect localization method that relies on the convolution relation (and deconvolution) between power port impulse responses, gate transients and power port transients for localizing defects in the chip. Simulations presented demonstrated that given the convolution relation and assuming accurate I_{DDT} measurements it is possible to diagnose and locate individual defective gates.

In [13] we proposed a similar approach based on deconvolution of power port transients for detection and localization of hardware security threats (Trojans) and demonstrated that given this relation it is possible to locate the intrusions with high accuracy and confidence.

As mentioned, in [11] there were some observable difference between SPICE simulations and convolution based calculated transients. Given the important implications and application of such a relation, it seemed necessary to provide further evidence on the fact that it hold true very accurately and can be relied on for future use. Therefore, in this work we have developed a new method for verifying this relation and through a series of simulations proved the existence and accuracy of convolution relation between gate transients, grid impulse responses and power port transients.

We also have made significant modification to the process of extracting paths from chip layout and performing simulations on individual paths. The outcome of this modified path extraction flow is more accurate SPICE models that include all parasitic components between the path and its neighbors in the chip layout. The more accurate SPICE models will in turn result in more accurate simulation results for gate transients which will improve the outcome of the convolution between gate transients and power grid impulse responses.

The rest of paper is organized as follows. Section 2 provides an overview of the path extraction method employed in [11] and the possible sources of inaccuracy that may have contributed to the differences in results of convolution process and those of SPICE simulations. Section 3 presents our new path extraction flow and discusses the improvements compared to the flow presented in [11]. It also discusses our approach to labeling gates of the sensitized path and running full chip simulations and calculating individual gate transients based on that. Section 4 presents our results obtained from the methods discussed in Sections 3 and compares them to those obtained in [11]. Papers ends with concluding remarks in Section 5.

2. Overview of Path Extraction Flow Reported in [11]

In [11], authors developed a path extraction tool for obtaining layout information of a desired path from layout of the whole chip. The extracted path layout was then taken through parasitic extraction to obtain a parasitic SPICE model. This model was then simulated and transients of individual gates of the path were recorded.

Another layout extraction tool is employed in [11] to extract the layout of the power grid by itself. The connection points of core's logic gates to the power grid are labeled before the extraction of power grid is performed. Impulse responses of the power grid from these connection point labels to each of the power ports are obtained by running SPICE simulations on the power grid model.

Convolution is performed using the power grid impulse responses and the individual gate transients to obtain the transients expected at the power ports of the full chip model. In order to validate this approach, SPICE simulations were also performed on the full chip model and the power port transients were compared to those obtained using convolution. It was shown that the

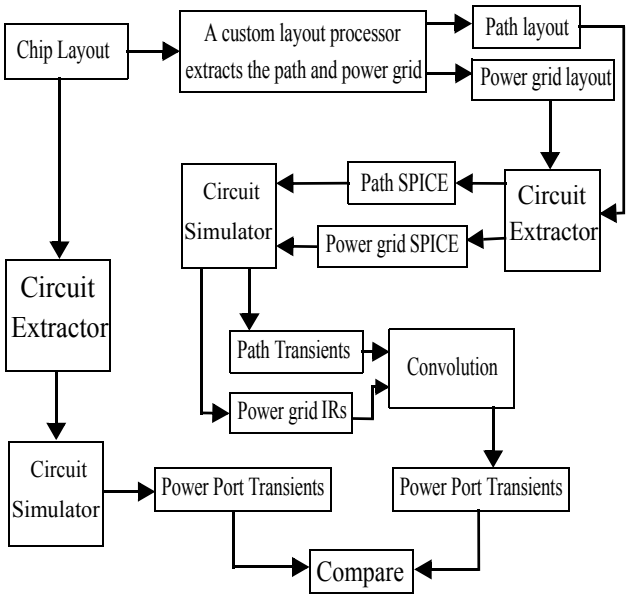

Fig. 1. Flow of path and power grid extraction implemented in [11]

two sets of transients were very similar. Figure 1 illustrates this flow.

The extraction flow employed in [11] results in some inaccuracy in the gate transients and power grid impulse responses, and hence in the power port transients calculated from the convolution of the two. The source of the inaccuracy originates in the use of the layout in the extraction process, i.e., a commercial circuit extractor is used to obtain the SPICE parasitic models of the grid and the path from the individual layouts. By separating the paths from the power grid first and then performing the circuit extraction, many of the coupling components between power grid and other parts of the chip are eliminated. The omission of these components results in some error in the calculated convolution outputs.

3. Modified Path Extraction and Path Labeling

In order to remove this source of error and verify the accuracy of the convolution relation, we developed another path extraction flow that is

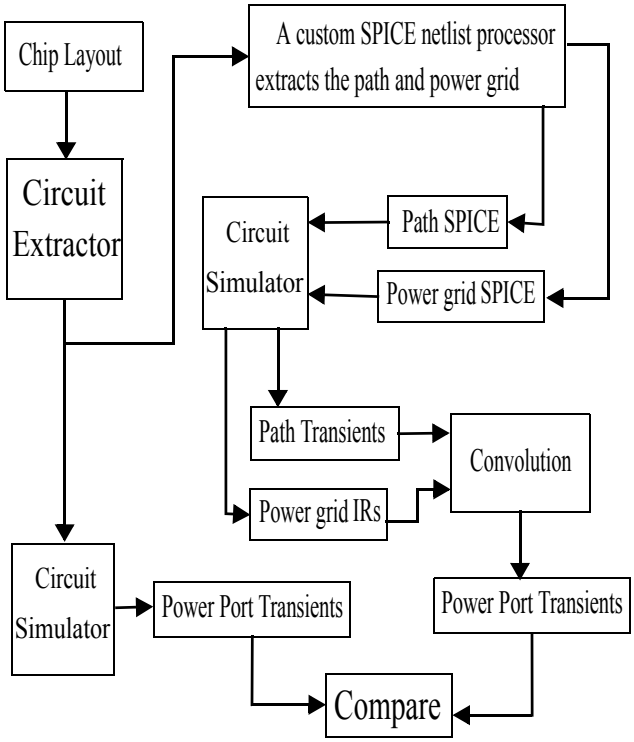

Fig. 2. Modified path extraction flow

shown in Figure 2Based on this flow, the layout of the entire chip is extracted using a commercial parasitic extraction tool to obtain the SPICE model. The parasitic SPICE model of the chip is then processed using a new extraction engine that produces separate SPICE models for power grid and the path. Resulting SPICE models include the main power grid resistive and capacitive components as well as coupling capacitances between the grid and the rest of the chip. Hence we expect higher accuracy for the results of the convolution of path transients and power grid impulse responses.

While we expected to observe significant improvements in the convolution results of path extraction flow shown in Figure 2 compared to the one in Figure 1, we decided to test and verify the existence of convolution relation in yet another experiment. We devised another flow shown in Figure 3 where instead of separating the path or power grid circuits from the chip model and then performing the SPICE simulations, full chip simulations were performed to obtain the path transients and the grid impulse responses. This is accomplished by labeling the connection points of the gates of the path to power grid and then running full chip simulations and recording

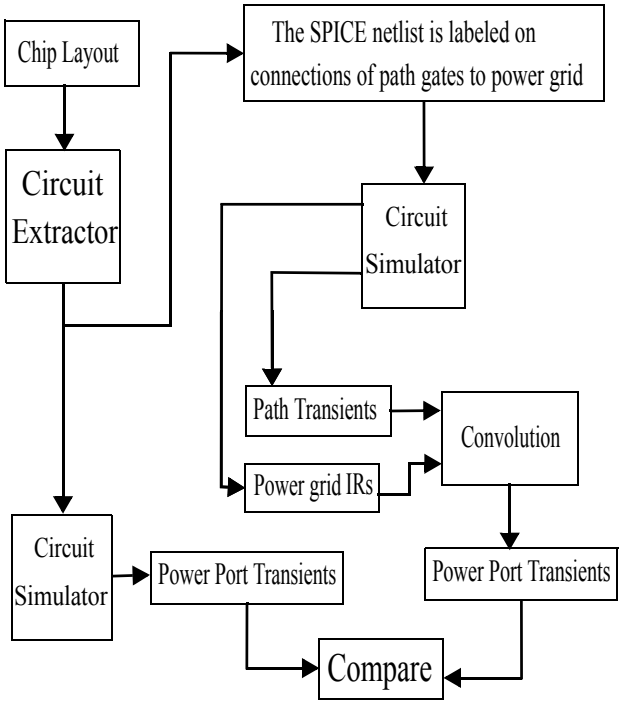

Fig. 3. Labeling the path connections to power grid and doing full chip simulations to examine the accuracy of convolution relation between path transients and power grid IRs.

the gate transients from the labels. The grid impulse responses are also obtained by applying impulse input to the labeled gate positions and measuring the power port outputs. Path transients and impulse responses obtained in this way are expected to be the most accurate because all the parasitic components of the chip are in place when the simulations are performed.

Bear in mind that the flow of Figure 3 involves full chip SPICE simulations, which is not possible for larger chips. Therefore, it will not serve the main purpose of [11] that is extraction of paths and simulating them individually and using convolution relation to obtain power port transient, thereby avoiding full chip SPICE simulations. However, it is employed here to examine the most accurate result that can be achieved using the convolution relation between gate transients and power grid impulse responses. These three methods are compared by using a full chip SPICE simulation (no convolution) as the reference.

4. Results

In a series of simulations, each of the three methods of obtaining path transients and power

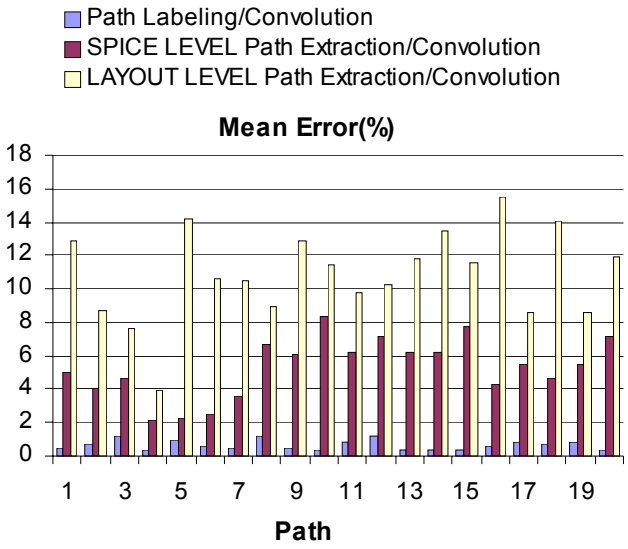

Fig. 4. Mean Error results for three methods of convolution-based calculation of power port transients.

grid impulse responses were employed for twenty different paths in C499 ISCAS benchmark. The path transients and power grid IRs were convolved and compared to the full chip SPICE simulation results. In order to compare the waveforms, three comparison metrics are defined and implemented, namely, mean error, correlation and timing error.

Mean error is defined in Equation 1 and specifies the average percentage of error for different nodes of the waveforms with respect to maximum value of the waveform.

$$\text{Mean Error} = \sum_{\text{waveform samples}} \left(\frac{||\text{SPICE\_Out}| - |\text{Conv\_Out}||}{\text{Total number of waveform samples}} \right) \quad \textbf{Eq.1.}$$

Figure 4 shows the mean error results for the three convolution-based power port transient calculation methods discussed, i.e. the layout level path extraction proposed in [11], the modified SPICE level path extraction depicted in Figure 2 and the path labeling approach shown in Figure 3. As seen in the figure, labeling the paths and doing SPICE simulation on the complete netlist of the chip to obtain the path transients and power grid IRs produces significantly more accurate waveforms compared to the other two methods. The modified path extraction method that is based on SPICE level netlist rather than the layout, improves the error level compared to layout level path extraction method. Table 1 summarizes

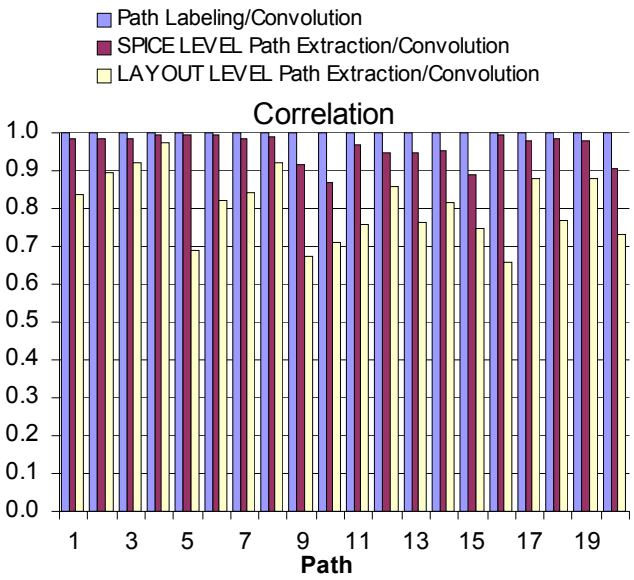

Fig. 5. Correlation results for three methods of convolution-based calculation of power port transients.

the mean and standard deviation of error for the methods.

	Path Labeling	SPICE Level Extraction	Layout Level Extraction
Mean	0.647	5.304	10.845
Std Dev	0.301	1.781	2.708

Table 1: Mean and standard deviation of error for the three path extraction methods

Correlation of the full chip SPICE simulation output and the convolution output waveform is calculated based on Equation 2 and is used as another measure of similarity between the waveforms..

$$\text{Corr\_Coef}(\text{SPICE\_Out}, \text{Conv\_Out}) = \frac{Cov(\text{SPICE\_Out}, \text{Conv\_Out})}{\sqrt{Cov(\text{SPICE\_Out}, \text{SPICE\_Out})Cov(\text{Conv\_Out}, \text{Conv\_Out})}}$$

$$Cov(x, y) = E((x - \mu_x)(y - \mu_y))$$

Eq.2.

Figure 5 shows the correlation results and Table 2 summarizes the mean and standard deviation of correlation for the three methods. Similar to results of the mean error, the correlation results demonstrate that labeling the paths and obtaining the path transients and power grid IRs generates waveforms with highest correlation to full chip SPICE simulation waveforms. Path extraction based on the circuit SPICE model stands in the middle and layout based path extraction method gives lowest correlations..

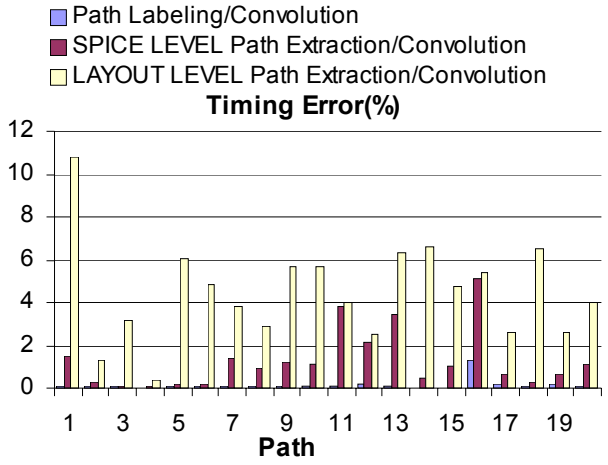

Fig. 6. Timing error results for three methods of convolution-based calculation of power port transients.

	Path Labeling	SPICE Level Extraction	Layout Level Extraction
Mean	0.999	0.961	0.807
Std Dev	0.001	0.038	0.090

Table 2: Mean and standard deviation of correlation for the three path extraction methods

Timing error is a parameter defined based on Equation 3 and is employed to investigate the timing difference between the two waveforms.

$$\text{Timing Error} = 100 \times \frac{(\text{SPICE\_Out Peak time - Conv\_Out Peak Time})}{\text{SPICE\_Out total time}}$$

Eq.3.

Figure 6 shows the timing error results for the methods and Table 3 summarizes the mean and standard deviation of the timing error. In this case, the path labeling approach still shows significantly lower error levels and the SPICE level circuit extraction introduces less timing error compared to layout level path extraction..

	Path Labeling	SPICE Level Extraction	Layout Level Extraction
Mean	0.135	1.278	4.504
Std Dev	0.269	1.364	2.302

Table 3: Mean and standard deviation of timing error for the three path extraction methods

Figure 7 shows two sample power port transients obtained based on the path labeling and the

SPICE level path extraction methods. The full chip SPICE simulation results are plotted for comparison.

As seen in the figure, transient waveforms obtained from the path labeling method (plotted in green) follow the accurate SPICE simulation results (plotted in red) very closely. Path extraction based on the SPICE model of the circuit results in waveforms that are close to the SPICE results but are distorted to some degree.

to summarize, both the error measurements reported above and the waveform samples shown in Figure 7 strongly suggest that labeling the paths and obtaining gate transients and then convolving these to impulse responses of power grid will produce waveforms that are almost identical to those generated by full chip SPICE simulations (Red and Green waveforms are very hard to distinguish in Figure 7). This is a clear proof of the fact that convolution relation hold true very accurately for the power grid. Results also show that our modified path extraction method has produced waveforms that are closer to those obtained from SPICE, compared to the ones calculated from the layout based extraction method reported in [11]. However, these results are not yet completely accurate and further improvements on the path extraction flow is required to obtain waveforms as close as possible to those of SPICE simulation.

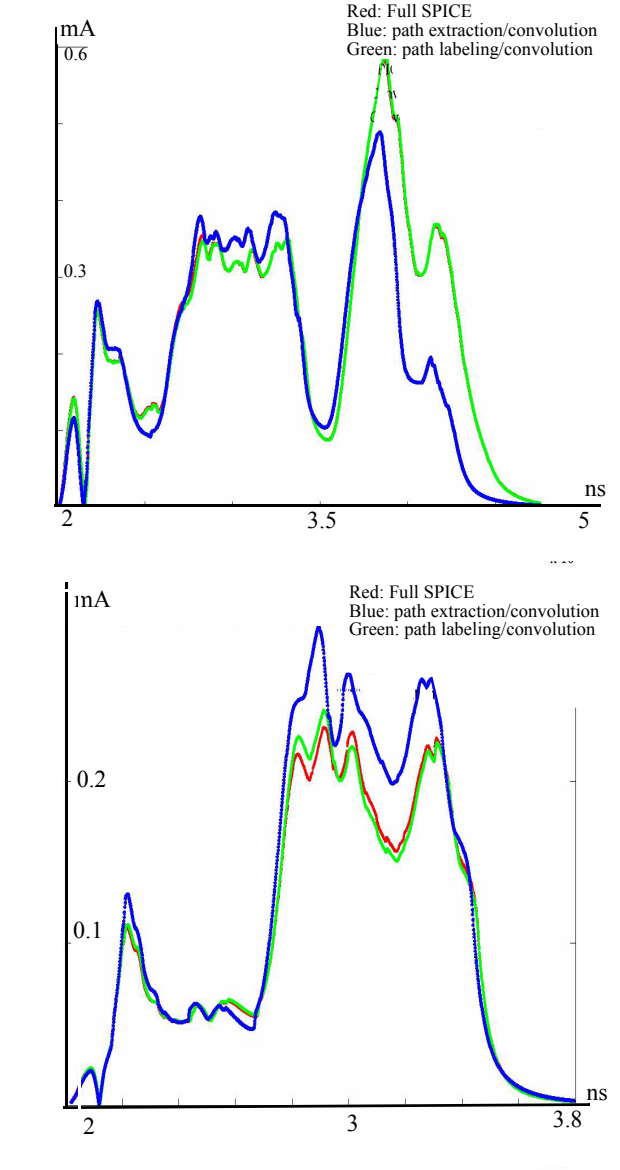

Fig. 7. Sample convolution based calculated transients and accurate SPICE transients

5. Conclusions

In this paper we presented our new method for extracting path circuit models from the full chip model. These models can be used to simulate each individual path rather than the whole chip. If power port transients of the chip are needed, as in many I_{DDT} test and diagnosis techniques, the individual gate transients can be convolved into the power grid impulse responses and the outcome will be very close to the full chip SPICE simulation. We have also presented our verification for the concept.

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