A Test Structure for Characterizing Local Device Mismatches

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Abstract

We present a test structure for statistical characterization of local device mismatches. The structure contains densely populated SRAM devices arranged in an addressable manner. Measurements on a testchip fabricated in an advanced 65 nm process show little spatial correlation. We vary the nominal threshold voltage of the devices by changing the threshold-adjust implantations and observe that the ratio of standard deviation to mean gets worse with threshold scaling. The large variations observed in the extracted threshold voltage statistics indicate that the random dopant fluctuation is the likely reason behind mismatch in the adjacent devices.

Introduction

Local device mismatches have short correlation distance. Characterization of random mismatches requires test structures with closely placed devices where each device can be measured individually. We describe a structure for statistical characterization of intrinsic parameter fluctuations in MOSFET devices. The test structure features a large array of densely populated SRAM sized devices. It allows fast and precise measurement of electrical characteristics of each individual device. The proposed structure is used to characterize the variations in device parameters for different threshold implantation levels in a 65nm SOI process [1]. The measurement results show that threshold voltage has a Gaussian distribution with its sigma/mean ratio higher for low channel doping. The random nature of the local device mismatch is also observed in the form of negligible spatial correlation in the measurement results.

Test Structure

Figure 1 shows the schematic of the test structure. The structure contains a 1250µm × 110µm array of small sized devices arranged in an individually addressable fashion. The array contains a total of 96,000 devices placed in 1,000 columns, with 96 devices in each column. To minimize parasitic effects, the gate-line and the drain-line of each column can be driven from both the top and bottom end of the column. The small height of the structure ensures that the worst case parasitic drop in a column line does not exceed 1 mV. The gate and drain-lines can also be sensed from both ends, which enable the measurement of voltages at the output of the column drivers. During the process of measurement, only one column is activated and the gate and drain terminals of the non-selected columns are clamped to their respective clamp voltages. The gate-clamp voltage can be chosen to drive the gate-lines of the non-selected columns with a negative voltage to minimize their leakage currents. Once a column is selected, the current steering circuit steers the current of the device under test (DUT) to the measuring pin and the currents of the remaining rows are steered to the sink pin. The current steering devices are made of thick oxide to reduce the gate leakage current. These steering devices lie in series between the source terminal of the DUT and the ground, causing the row voltages to rise slightly above the ground. The parasitic resistance of the wire also adds an additional resistance between the source node of the DUT and the steering device. To account for these IR drops, sense capability is added to measure the row voltages at both ends of the array. As shown in Figure 2, the setup steers all current in the left direction, hence the sense voltage at the right-end is used as a measure of the exact voltage appearing at the source node of DUT. The difference between the sense voltages at two ends of a row can also be used as an indicator of the IR drop due to parasitic resistances. *Level Sensitive Scan Design* (LSSD) latch banks are placed at all four sides of the array. The top and bottom banks are used to select the column under test, as well as to place non-selected columns to the clamp voltage. The left and right banks set up proper measure, sink and row-sense for each row. The impact of channel doping on random dopant fluctuation is studied by including devices with different V_T implants in the array.

Experimental Measurements

The manufactured dies were packaged using flip-chip technology and were interfaced with a measurement instrument through a test board. Table I lists key features of the test chip and Figure 3 shows the layout and a picture of the test-board. All measurements were taken in a thermal chamber at a controlled temperature and an on-chip thermistor was used to monitor temperature during measurements. The sum of currents due to non-selected DUTs in a row was measured to be negligible. However, for precise leakage measurement, each row was calibrated by measuring the current through that row when no device was selected. The measured electrical characteristics of a sample device are shown in Figure 4. Figure 5 shows the subthreshold leakage histogram of low threshold devices as obtained from the measurement of 8640 such devices in the array. The subthreshold leakage shows a lognormal distribution due to its exponential dependency on the threshold voltage variation. Figure 6 shows a spatial map of the subthreshold leakage and Table II shows the results of correlation analysis between the leakage and the physical distance. The large *p-values* in the table indicate very low confidence that the correlations are deterministic. The lack of spatial correlation suggests that the random dopant fluctuation is likely to be the main contributor of local device mismatch [2],[3].

The devices with different threshold-adjust implantations were fully characterized by taking a large set of electrical measurements. The measured statistical data was mapped into statistics of device parameters through parameter extraction process. A physical model based on Reference [4] was used as the underlying model. Figure 7 shows the extracted threshold voltage distribution of one set of devices. The figure shows that the threshold distribution is Gaussian in nature with a significantly large spread around its mean value. Figure 8 reports the standard deviation to mean ratio for devices with different threshold implantation levels. The figure shows that the sigma/mean ratio is worse for low threshold devices. This result suggests that the impact of threshold variability will continue to grow with scaling. A similar analysis of subthreshold slopes is reported in Figures 9 and 10. The measurements indicate that higher doping results in better subthreshold slope due to reduced DIBL effect. However, the standard deviation numbers were observed to be fairly independent of the nominal doping density.

Conclusion

We demonstrated a test structure to enable statistical characterization of device parameters. The measured results can be used to analyze the impact of local device mismatch on stable operation of SRAM cells. The measured variation data and its random nature demonstrate the significance of device mismatch and indicate the importance of variability characterization test structures.

References:

[1] E. Leobandung *et al.*, *VLSI Tech Symp*, pp. 126-127, 2005.
[2] M.J. Pelgrom *et al.*, *JSSC*, pp. 1433-1440, 1989.
[3] T. Mizuno *et al.*, *TED*, pp. 2216-2221, 1994.
[4] R.V.H. Booth, *BMAS*, pp. 39-44, 2001.

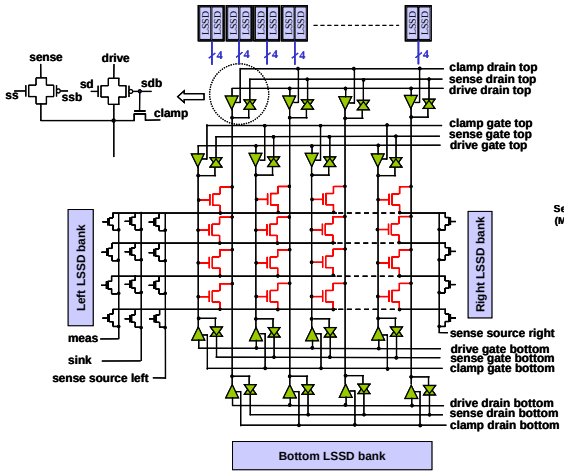


Fig 1: Schematic diagram of the test structure

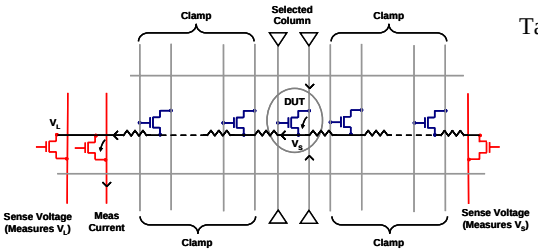
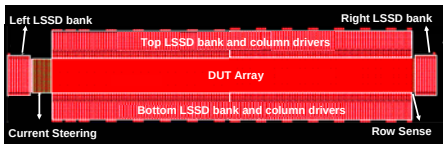


Fig 2: Row sensing for IR drop calibration

Table I: Test Chip Details

SOI Technology	
Gate Length	35nm
Gate Oxide	1.05nm
Cu Metal	10 levels
Structure	
Devices	96,000
DUT area	0.1375 mm^2



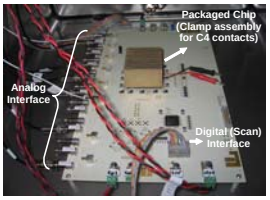
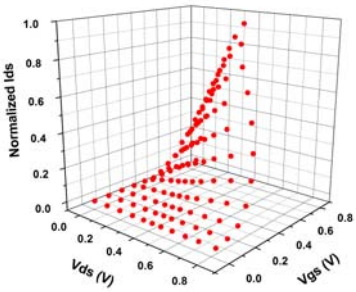


Fig 3: layout of the structure and picture of the test board



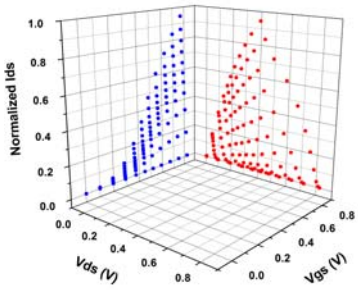


Fig 4: Measured I-V surface of a sample device and its corresponding Ids-Vds and Ids-Vgs projections

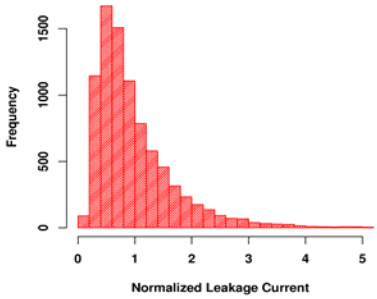


Fig 5: Measured leakage histogram

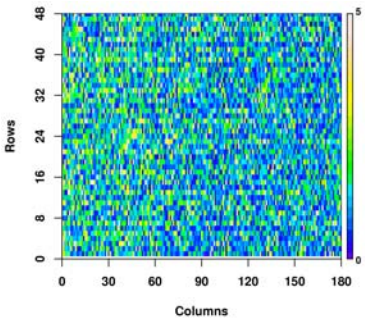


Fig 6: Spatial leakage distribution

Table II: Correlation analysis as a function of spatial distance

Direction	Correlation Coefficient	p-value
Vertical	-0.0927	0.2158
Horizontal	-0.1278	0.3865
Arbitrary	-0.0119	0.5507

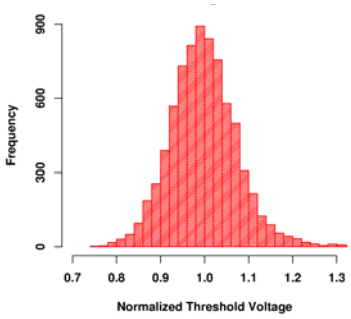


Fig 7: Threshold voltage distribution

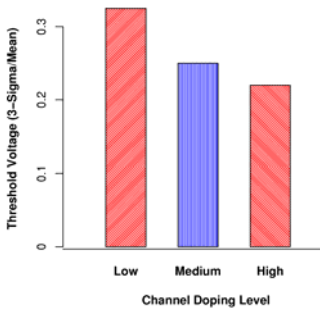


Fig 8: Threshold voltage statistics for three different V_T implants

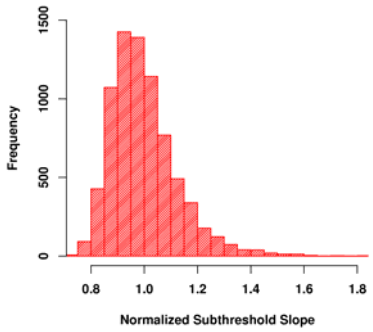


Fig 9: Subthreshold slope distribution

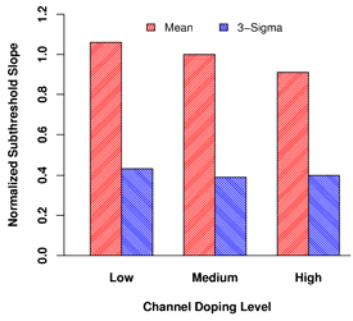


Fig 10: Subthreshold leakage statistics for three different V_T implants