IC Diagnosis Using Multiple Supply Pad I_{DDQ}s

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A I_{DDQ} technique is proposed based on an extension of a V_{DDT}-based method called transient signal analysis. The method, called quiescent signal analysis, uses I_{DDQ}s measured at multiple supply pins as a means of localizing defects.

I_{DDQ} has been used extensively as a reliability screen for shorting defects in digital integrated circuits. Unfortunately, single-threshold I_{DDQ} methods applied to devices fabricated in deep-submicron technologies result in unacceptably high levels of yield loss. The significant increase in subthreshold leakage currents in these technologies makes it difficult to set an absolute pass/fail threshold to fail only defective devices.[1] There have been proposed solutions to the subthreshold leakage current problem and, more recently, to process variation issues. Current signatures, delta-I_{DDQ} and ratio I_{DDQ} are based on a self-relative analysis, in which the average I_{DDQ} of each device is factored into the pass/fail threshold value.[2–4] We refer to the technology dependency of subthreshold leakage current as a technology-related variation effect to contrast it with the chip-to-chip variation effects caused by changes in process parameters (process variation).

We base our approach on a previous V_{DDT}-based method called transient signal analysis (TSA).[5] TSA uses regression analysis to calibrate for process and technology-related variation effects by cross-correlating multiple supply pin transient signals measured under each test sequence. The I_{DDQ} signal analysis, or QSA, method proposed uses a set of I_{DDQ} measurements instead, each obtained from the individual supply pins of the device under test (DUT). The process and technology calibration procedure used in QSA is based on a regression analysis procedure similar to TSA.

In TSA, we referred to signal variation resulting from defects as regional variation, to contrast it with the global variations introduced by process and technology-related effects. For transient signals, the supply rail's resistance-capacitance (RC) network modifies signal characteristics, such as phase and magnitude, at different supply pin test points. In QSA, only the resistive component of the supply rail network introduces variation in the I_{DDQ} values at different supply pins. In either case, the position of the defect in the layout with respect to any given power supply pin is related to the amount of regional defect variation observed at that pin. For QSA, the variation is directly related to the resistance between the defect site and the pin. For example, a larger value of I_{DDQ} is expected on supply pins closer to the defect site because of the smaller resistance. Therefore, the multiple I_{DDQ} measurements can be used to detect the defect as well as triangulate the physical position of the defect in the layout.

Defect detection experiments are on going and will be addressed in a future work. In this work, we develop a diagnostic method for QSA and present a set of simulation results are to demonstrate its defect localization accuracy. A

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proposed characterization procedure can be performed beforehand to determine the mapping between resistance and distance in the layout. Our results show that, on average, the x,y layout prediction given by the method is within 6% of the actual defect location in 2 um technology and within 10% for 0.5-micron technology. This suggests that the technique is best used in combination with fault dictionary techniques as a means of further resolving the defect's location.

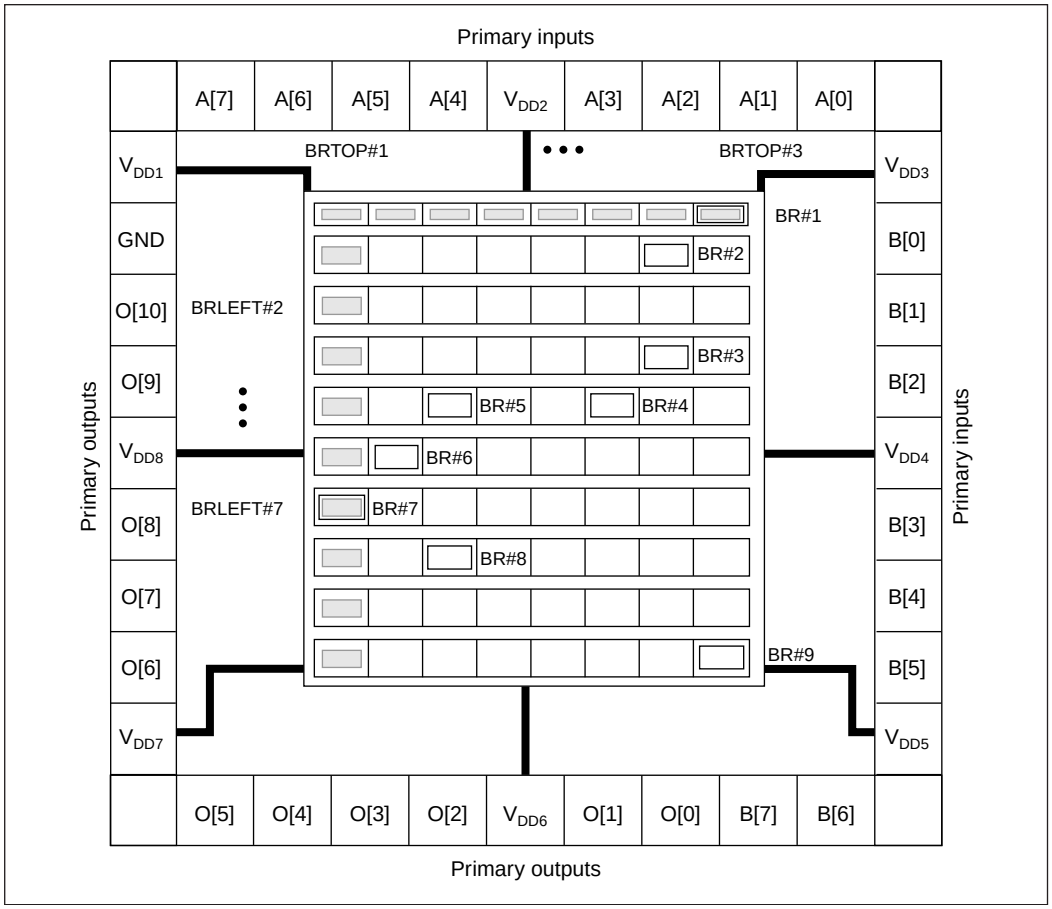

Figure 1. The layout of the 8-bit multiplier with resistive bridging defects.

Background

Several diagnostic methods have been developed based on I_{DDQ} measurements. In general, these methods produce a list of candidate faults from a set of observed tester failures using a fault dictionary. Several statistical algorithms can determine the likelihood of each candidate fault. For example, signature analysis uses the Dempster-Shafer theory, which is based on Bayesian statistics of subjective probability.[6] Delta I_{DDQ} makes use of the concepts of differential current probabilistic signatures and maximum likelihood estimation.[7] Although these methods are designed to improve the selection of fault candidates, in many cases, they are not able to generate a single candidate. Other difficulties of these methods include the effort involved in building the fault dictionary and the time required to generate the fault candidates from the large fault dictionary using device tester data.

The QSA procedure proposed here can help in the selection of the most likely candidate from the candidate list produced by these algorithms. The physical layout information generated by our method can be used with information that maps the logical faults in the candidate list to devices in the layout. In addition, it may be possible to use the (x,y) location information provided by QSA as a means of reducing the search space for likely candidates in the original fault dictionary procedure. This can reduce the processing time and space requirements significantly.

Experimental Design

QSA experiments were conducted on a full-custom design of an 8-bit two's-complement multiplier. A block diagram of this device is shown in Figures 1 and 2. The primary inputs, labeled A[0] through A[7] and B[0] through B[7] are shown along the top, right, and bottom of the figure. Only ten of the primary outputs are wired to the pad frame (and observable at the package pins of the device.) The power

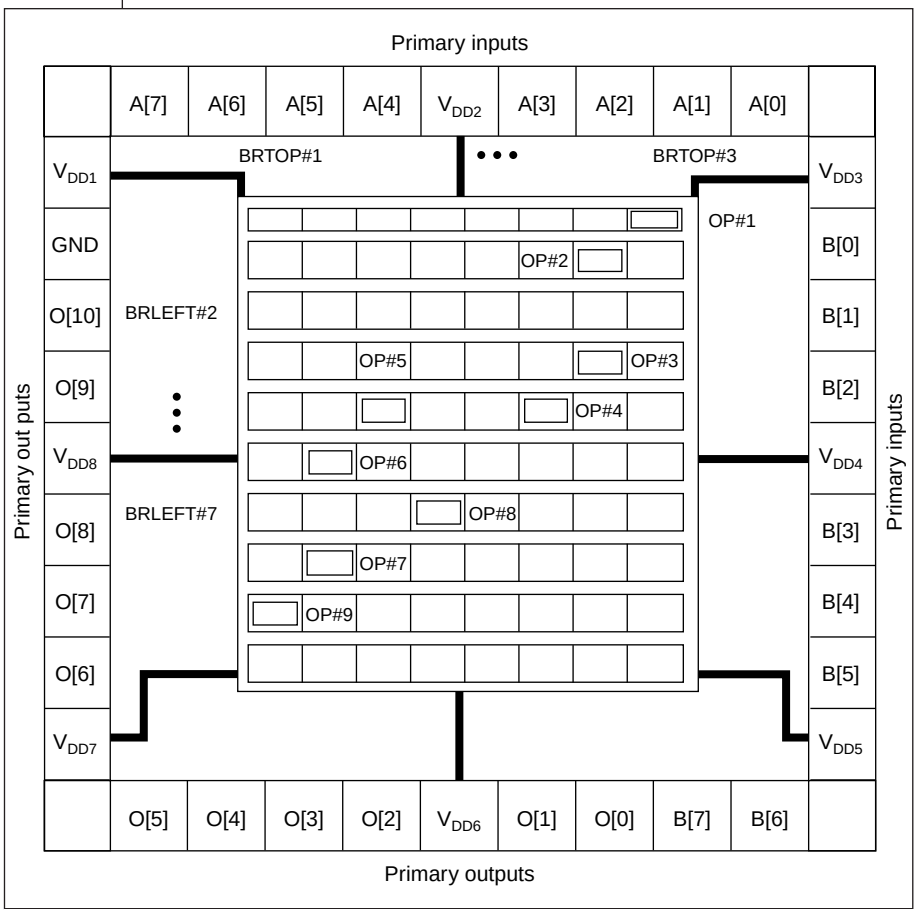

Figure 2. The layout of the 8-bit multiplier with resistive open defects.

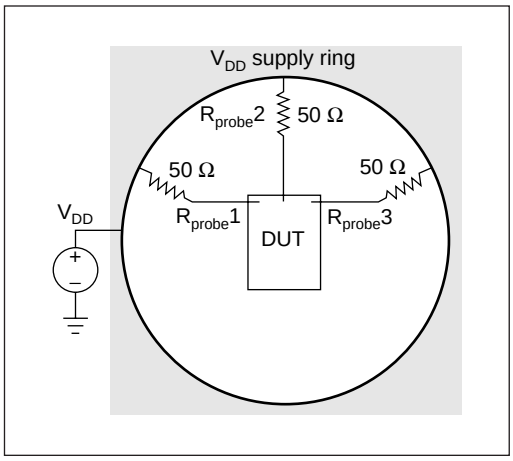

Figure 3. Probe card model.

supplies for the core logic are labeled as V_{DD1} through V_{DD8} and are distributed evenly along the periphery of the core logic. The core logic consists of a rectangular array of AND gates and full adders, shown as rectangles in the center of the figure. Resistive bridging (Figure 1) and open (Figure 2) defects were inserted into these cells at the labeled locations in the figure. Nine of the bridging defects and the open defects were distributed throughout the layout. Fifteen additional bridging defects were placed in cells along the top and left sides. We used the SPACE extraction tool to generate RC models from the layout.[8]

Two methods are used to measure the individual I_{DDQ} values at the supply pads shown in these figures. In a Spice simulation environment, the most straightforward method is to use the V_{DD} branch currents of the ideal sources directly. For production test, this corresponds to using the tester electronics at wafer probe to monitor a set of power supplies that drive each of the V_{DD} pads. This may not be possible due to tester limitations on available power supply channels. Therefore, a second method based on voltage measurements is proposed. At wafer probe, it is possible to measure the current as a voltage drop by inserting series resistors between the supply pads and the supply ring on the probe card, as shown in Figure 3. The value of the series resistance (50 ohms in our experiments) depends on the average steady-state current drawn by devices in the process. It may be necessary to switch out the resistors to prevent excessive supply rail voltage drops, when the DUT is switched between states.

Experimental Method

Simulations were carried out on circuit models derived from a 2.0-micron n-well technology. In this technology, background currents were very small (~30 nA) and are not accounted for directly. However, we later describe several extensions of the method that calibrate for significant leakage currents associated with current technologies.

Phase 1: Resistance Network Analysis

The objective of this phase is to determine the equivalent resistances (R_{eqi}) between the supply pads (V_{DDi}) and the point where the defect draws current from the supply grid. The R_{eqi} are labeled R_{eq1} through R_{eq8} in Figure 4. The R_{eqi} are computed by setting the state of the circuit such that the short is provoked and the volt-

ages at each of the supply pads are measured. Under this condition, the defect will draw current from each supply pad proportional to the value of the R_{eq}. As explained previously, the 50 ohms (R_{probe}) placed in series with the supply pad probes allows the currents to be measured as voltage drops in this work. If the appropriate measurement instrumentation is available, I_1 through I_8 can be obtained directly.

Figure 5 shows supply pad voltages from a device simulation with an inserted defect, as shown in Figure 4. The vertical displacement of the waveforms along the right portion of the figure indicates that the defect causes a regional current variation in the device. The magnitude of the voltage drop (from V_{DD}) of each of the waveforms in Figure 5 is inversely related to the R_{eq} between the supply pads and the defect site. Therefore, the supply pads with the largest voltage drops indicate they are in close proximity to the defect. Although it is unlikely that the relationship between resistance and distance is strictly linear and uniform along all directions from the supply pads to points in the layout, it is certainly valid to assume it approaches such a function if the supply topology is grid-like and regular. Good results are obtained under this assumption for our experimental circuit.

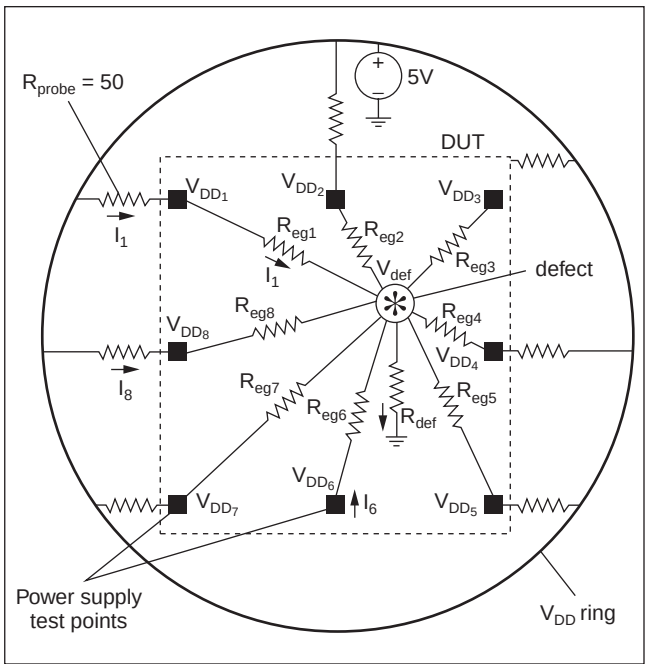

Figure 4. Equivalent resistance network with defect inside the circuit.

Since the I_{DDQ} values are related only to resistive components of the network, as shown in Figure 4, the following system of equations can be written to describe their behavior. The I_i variable represents the branch currents through each of the supply pins, R_{probe} is known (50 ohms in our experiments), and R_{eqi} are the unknowns.

$$I_i \times (R_{eqi} + R_{probe}) = V_{DD} - V_{def}$$
$$i = 1...8$$

The voltage at the defect site (V_{def} at the star in Figure 4) is also unknown but can be used as the point of reference for the system of equations. This formulation yields eight equations and nine unknowns. Therefore, without additional information, we cannot determine the R_{eqi}. However, the important information is

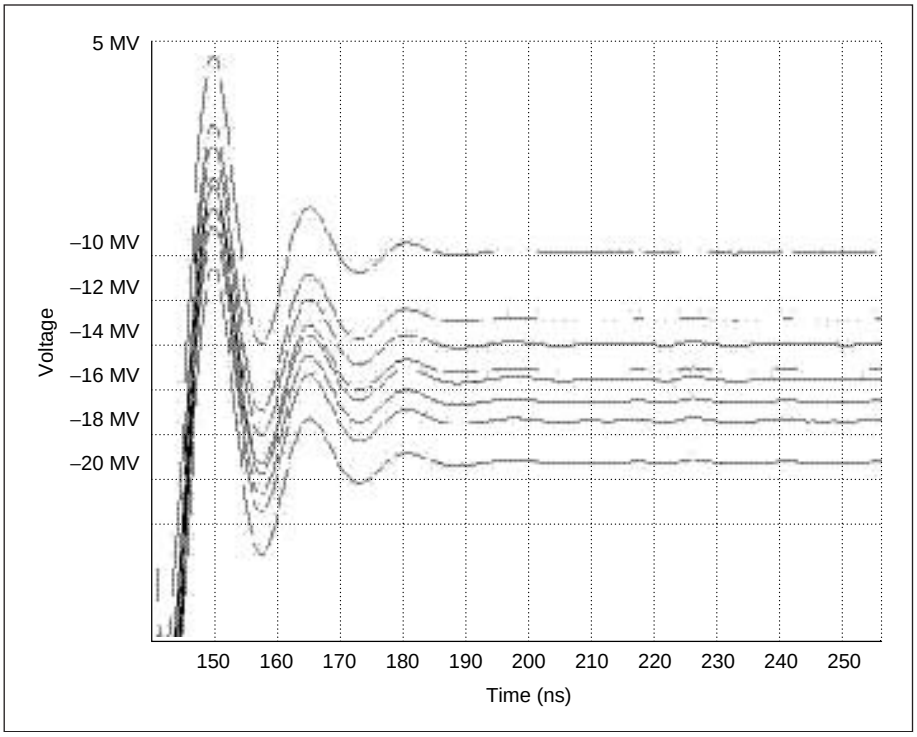

Figure 5. Voltage waveforms measured at the eight supply pins with the shorting defect provoked.

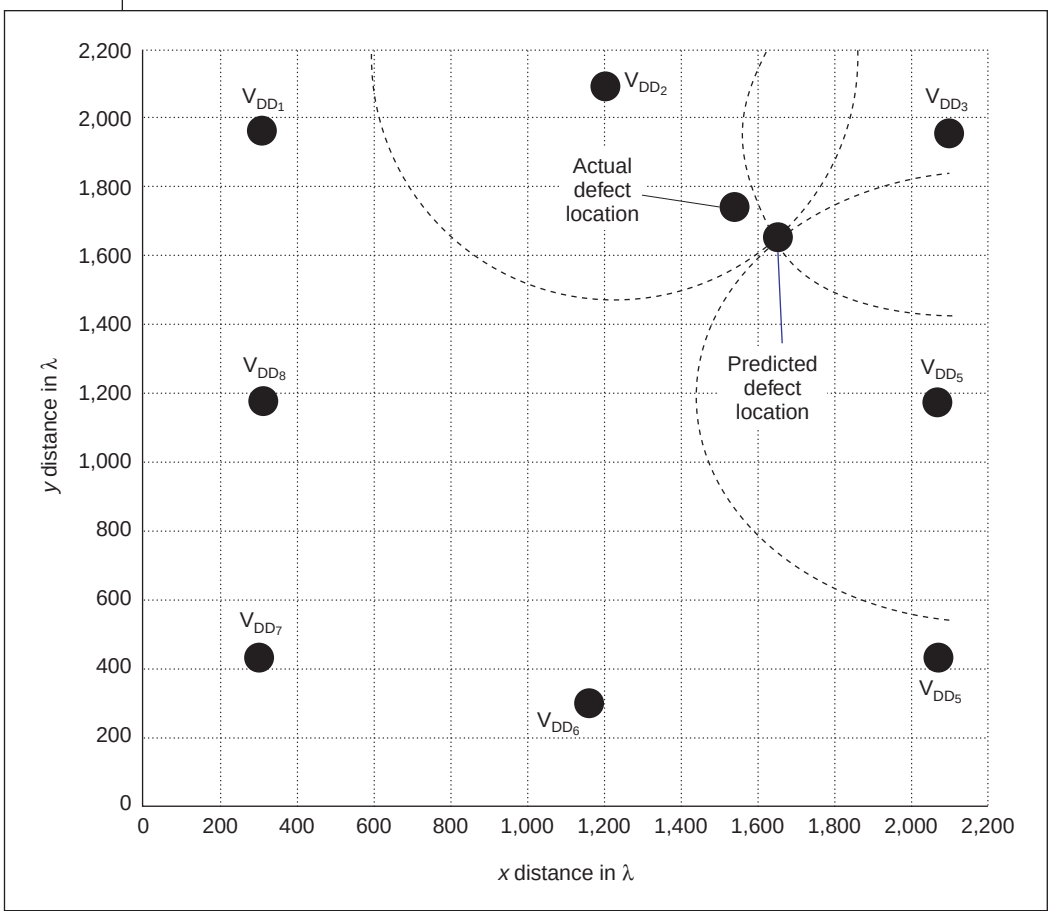

Figure 6. Bridging experiment 1 using localization method 1.

the relative differences between R_{eqi} and not the absolute value. This relationship is captured by computing ratios. As described next, the ratios can be scaled as easily as the real R to obtain the location of the defect. The ratios of resistances R_{eq1} to R_{eq8} are computed from the equations given in Equation 2 below.

$$I_i \times (R_{eqi} + R_{probe}) = (R_{eqk} + R_{probe})$$
$$R_{ratioi} = \frac{I_k}{I_i} \times R_{eqk} + \left(\frac{I_k}{I_i} - 1\right) \times R_{probe}$$
$$for\, i = 1...8 \, excluding \, k$$

These equations express seven of the R_{eqi} as a function of the eighth. Any R_{eqk} can be chosen as the reference resistance.

Phase 2: Resistance-to-Distance Analysis

The objective of this phase is to map from R_{ratioi} to a set of distances in the layout, each directed from a supply pad to the defect site. In the ideal case, the resistances scale linearly to distance uniformly along any vector. However, complex and/or irregular supply topologies routed in multiple metal levels with resistive contacts connecting them, can complicate the resistance to distance mapping function. There are two mapping functions; one assumes linearity and a second handles more complex functions.

Method 1

This method simply uses the resistance ratios as distance ratios, which are scaled by a common factor as a means of finding a point of intersection among them.

Step 1. Select the supply pad V_{DDk} closest to the defect site. This is equivalent to selecting the largest current value, I_k or the minimum resistance, R_{eqi} in the second equation. Since the distance d_i, between V_{DDi} and the defect site is assumed proportional to R_{eqk}, V_{DDk} is closest and is referred to as the primary supply pad.

Step 2. Select the supply pads with the second and third largest current values. These pads are likely neighbors of the primary supply pad. If the supply pad configuration is similar to the one shown in Figure 1, it is possible that these choices result in a line of pads along one dimension of the layout. For example, if supply pads V_{DD3}, V_{DD4}, and V_{DD5} are selected in the design shown in Figure 1, only the y dimension is covered. In this

case, the supply pad that ranks fourth in the sorted list of supply currents should be selected instead (V_{DD2} since it covers the x dimension). Similar heuristics can be used for other supply pad configurations.

Step 3. Using the three selected supply pads, establish a set of circles with radii proportional to the ratios computed in the second equation. An iterative algorithm is then applied that scales the radii by the same factor and tests for intersection. The point of intersection indicates the x,y location in the layout at which the defect draws current from the supply grid.

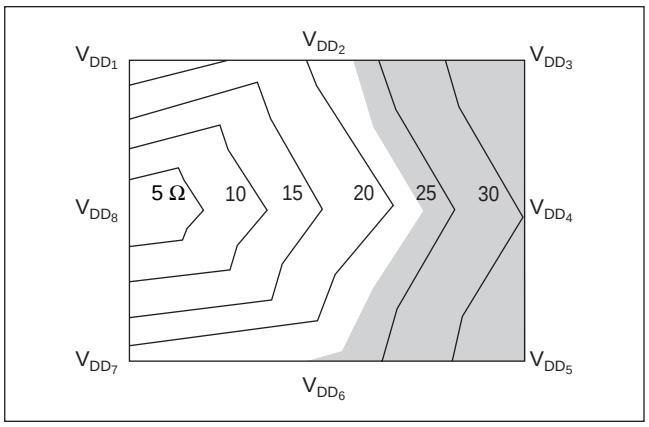

Figure 7. The resistance-to-distance mapping contour for V_{DD1}.

An application of this method is shown in Figure 6 for bridging experiment 1. The figure represents the layout of the multiplier with the x and y scales given in units of lambda. The supply pad locations are labeled along the edges of the figure. Three dashed circles are shown in the upper right hand corner centered around the supply pads V_{DD2},V_{DD3}, and V_{DD4}. These supply pads were selected because they sourced the largest currents, as given in Steps 1 and 2 in the method. The circles have been scaled so that they have a common point of intersection. The predicted and actual (x,y) locations are labeled in the figure.

Method 2

The second method uses a contour to map resistance to distance in the layout. Since the actual mapping function is not easily obtained, this estimate is designed to provide a more accurate prediction for supply grid designs with irregular topologies. The data to construct the contour can be obtained easily using a defect-free device or a simulation model.

The method is also based on equivalent R_{eqi}, but additionally considers the R_{eqi} between the supply pads themselves. The latter are computed for any reference supply pad and other supplies by setting the reference supply pad to a voltage slightly less (such as 100 mV) than the nominal supply voltage. The remaining supply pads are set to their nominal voltage and the currents measured. The distance between each pairing of supply pads is easily obtained from the layout. The ratio of distance and resistance defines the scaling factor along each of the vectored directions from the reference supply pad to the other supply pads. The experiments produce a set of contours (one for each supply pad) that are used instead of the circles in the localization procedure described for Method 1.

This method simulates the presence of a defect at each of the supply pads. Therefore, the R_{eq} obtained from the measurement accurately reflects the resistance for defects in the vicinity of that supply pad. The drawback of contours is that they may produce several different points of intersection under different scaling factors. Therefore, several predicted locations may be generated by the algorithm described in method 1.

Figure 7 shows the contour obtained for V_{DD8} in our experiments. The lines representing the contour are each labeled with the R_{eqi} they define at points in the layout under their curve. A full set of contours would consist of one such mapping for each supply pin. Figure 8 (next page) shows the method applied to the resistance data obtained for bridging experiment 1. In comparison to the localization result shown in Figure 6, only slightly better results are obtained for this experiment using contour maps.

Experimental Results

The experimental results are reported as (x,y) coordinates giving the predicted and actual defect locations and the error in the predictions. The error is computed as the directed

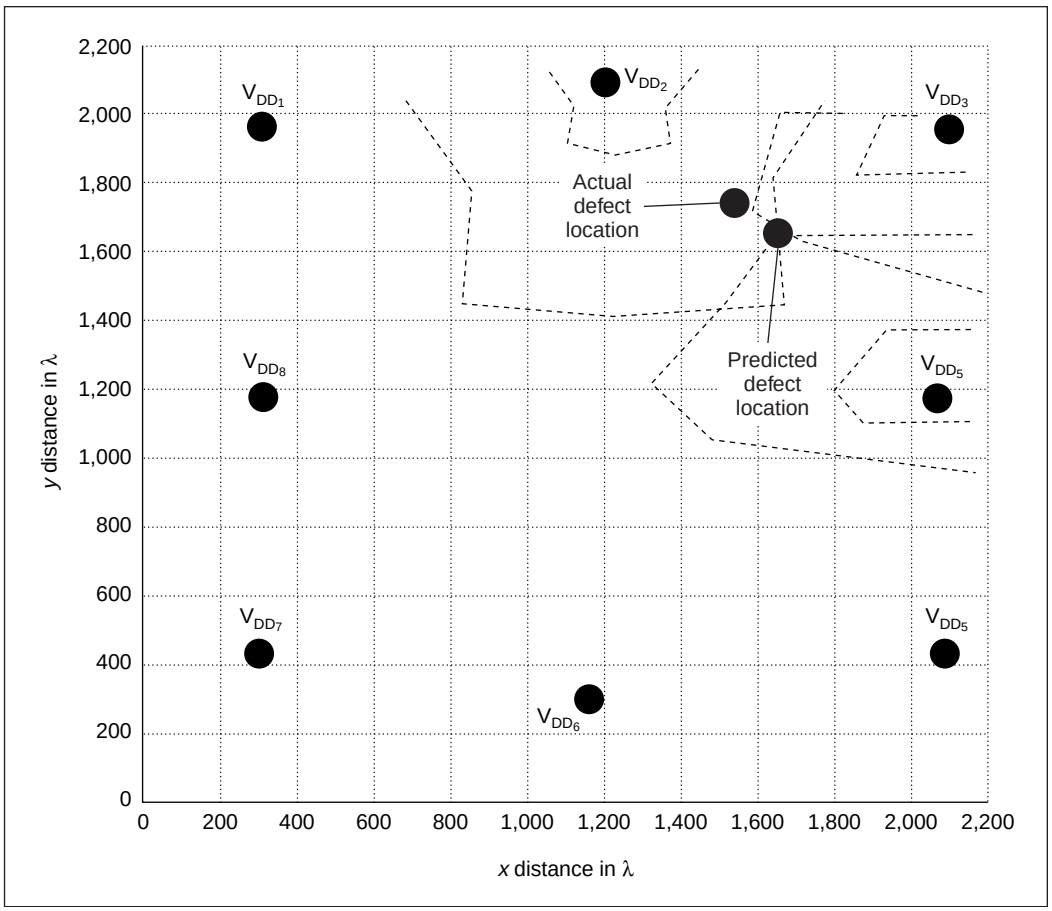

Figure 8. Bridging experiment 1 localization using contour maps (method 2).

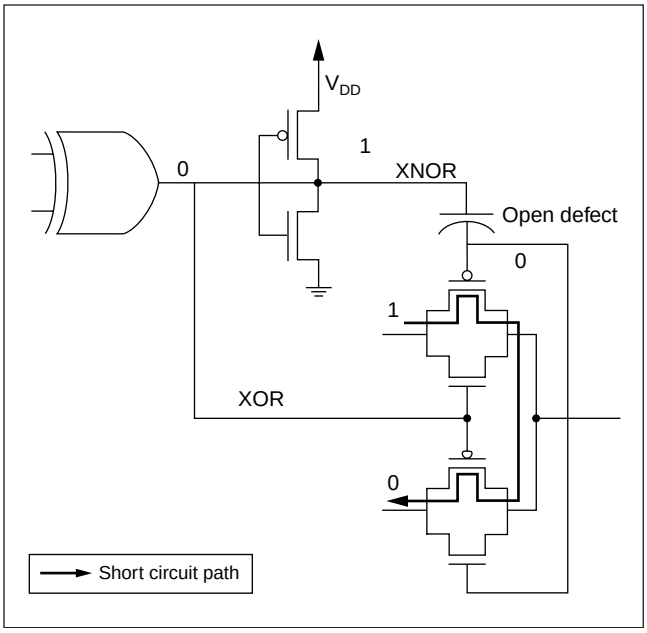

Figure 9. A portion of the transmission gate full adder, illustrating the shorting behavior caused by an open defect.

distance between the predicted and actual locations divided by the width of the layout using:

$$\frac{\sqrt{(x_{predict} - x_{actual})^2 + (y_{predict} - y_{actual})^2}}{\text{width\_of\_layout}} \times 100$$

The localization curves for bridging experiment 1 are shown in Figures 6 and 8 and described in the previous section. The error for this experiment is approximately 7% using either resistance-to-distance method 1 or 2.

Figure 9 shows a portion of the transmission-gate full adder schematic used in the design. The implementation uses a 2-to-1 multiplexer whose select lines are driven by an XOR gate and an inverter. The open is shown at the output of the inverter. The undriven node floats to 0 V leaving the p-channel transistor in the upper transmission gate permanently on. Under a circuit state that causes the XOR to output a 0, the opposing values on the inputs to the multi-

plexer create a short, as shown by the thick line in the figure. Figure 10 shows the results from this experiment in graphical form. The actual and predicted locations are indicated in the figure using supply pad test points V_{DD6}, V_{DD7}, and V_{DD8}.

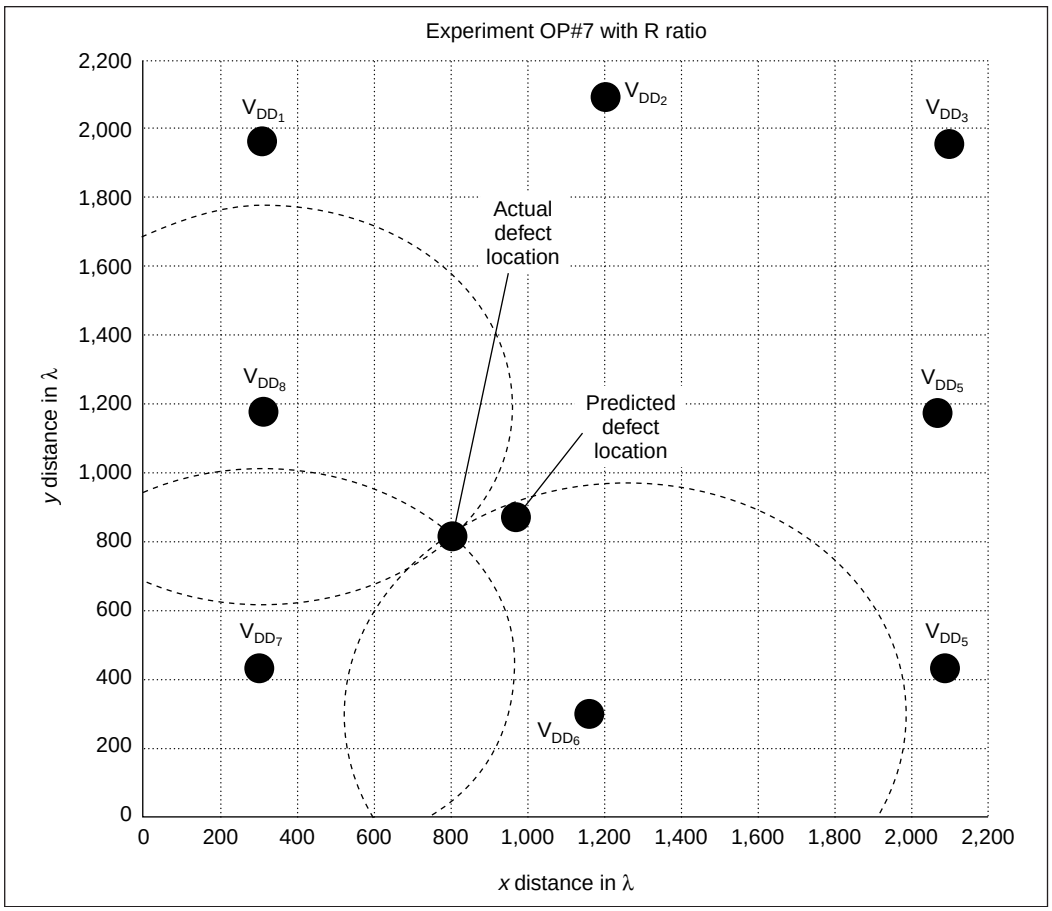

Figure 10. Open experiment 7 results using localization method 1.

A summary of the prediction errors for the experiments is given in Table 1 for simulations on the multiplier in 2-micron n-well technology. The results of simulations in 0.5 um n-well technology are shown in Table 2. In each table, the leftmost column identifies the experiment. The second column gives the actual position of the defect in the layout (in units of lambda), and the third column gives the predicted location. The last column gives the prediction error computed using equation 3. The width of the layout is 2,200 lambda.

As indicated in Table 1, only three of the open defects were diagnosable. This was possible because the floating node under experiments OP#3, OP#7, and OP#9 caused a shorting condition between V_{DD} and GND in downstream gates, as shown in Figures 9 and 10.

The rightmost column of Table 1 indicates that the worst-case error is less than 10%. For example, the errors for BR#2 and OP#7 are 9.9% and 9.86%, respectively. The mean error is about 6%. We expect that inaccuracies in the extracted model and simulation tolerances are responsible for a portion of this error. However, the error is small enough to suggest that this procedure provides valuable diagnostic information for fault dictionary techniques.

The results obtained so far under the 0.5-micron model indicate that the prediction errors are somewhat larger, with the average approximately 10% and the worst case at 12.6%. This is unexpected since the increase in the supply rail resistance should improve the resolution of the method (assuming that the transistor betas are similar to the 2.0-micron design). Again, model extraction inaccuracies and simulation error are the likely candidates for this discrepancy and are under investigation.

Process Variation and Leakage Current

The background leakage currents measured in the simulation experiments (< 30 nA) were very small. However, in deep-submicron technologies, these currents are orders of magnitude higher and must be accounted for. In this section, we describe a regression analysis procedure for QSA that can be used to calibrate for background currents. The method is adapted

Table 1. Two-micron experiment results.

Defect	Actual location	Predicted location	Error in 2-microns (%)
BR#1	(1540,1736)	(1640,1640)	6.3
BR#2	(1465,1600)	(1600,1625)	7.1
BR#3	(1465,1365)	(1580,1550)	9.9
BR#4	(1325,1240)	(1600,1630)	6.5
BR#5	(1120,1240)	(1173,1215)	2.6
BR#6	(1020,1120)	(1150,1210)	7.1
BR#7	(912,993)	(770,835)	9.5
BR#8	(1110,875)	(1190,877)	3.6
BR#9	(1560,712)	(1657,625)	5.9
OP#3	(1410,1442)	(1580,1550)	9.1
OP#7	(962,914)	(760,835)	9.86
OP#9	(903,790)	(735,800)	7.65
BRtop#1	(800,1705)	(760,1706)	1.8
BRtop#2	(900,1705)	(804,1710)	4.4
BRtop#3	(1000,1705)	(854,1670)	6.8
BRtop#4	(1110,1705)	(1165,1770)	3.87
BRtop#5	(1230,1705)	(1194,1728)	1.94
BRtop#6	(1340,1705)	(1524,1678)	8.45
BRtop#7	(1450,1705)	(1554,1652)	5.3
BRtop#8	(1560,1705)	(1605,1678)	2.38
BRleft#2	(790,1630)	(808,1630)	0.82
BRleft#3	(790,1515)	(832,1580)	3.5
BRleft#4	(790,1393)	(844,1510)	5.8
BRleft#5	(790,1272)	(910,1165)	7.3
BRleft#6	(790,1152)	(910,1155)	5.45
BRleft#7	(790,1032)	(750,825)	9.58
BRleft#8	(790,918)	(745,805)	5.53

Table 2. 0.5-micron experiment results.

Defect	Actual location	Predicted location	Error in 2-microns (%)
BR#1	(1540,1736)	(1660,1945)	10.68
BR#2	(1465,1600)	(1665,1705)	10.27
BR#3	(1465,1365)	(1248,1370)	9.7
BR#4	(1325,1240)	(1448,1190)	6.0
BR#5	(1120,1240)	(1163,1020)	10.19
BR#6	(1020,1120)	(1143,1205)	6.6
BR#7	(912,993)	(1145,885)	11.6
BR#8	(1110,875)	(1160,613)	12.1
BR#9	(1560,712)	(1620,501)	10.0
OP#3	(1410,1442)	(1255,1355)	8.08
OP#7	(962,914)	(750,735)	12.6
OP#9	(903,790)	(730,698)	8.9

from the procedure defined for TSA.[5]

The defective device I_{DDQ} consists of two components, the current drawn by the defect, and the process and technology-related leakage current, such as subthreshold leakage current. This changes the formulation presented in Equation 2 to that shown in Equation 4.

$$(I_{leakagei} + I_{defecti}) \cdot (R_{eqi} + R_{probe}) = (I_{leakagek} + I_{defectk}) \cdot (R_{eqk} + R_{probe})$$

The leakage current is given as a set of currents, $I_{leakagei}$, in the equations, each representing the current drawn through each of the supply pins. If the transistor density in the layout is regular, then the leakage current will be evenly distributed among the supply pins, yielding a single value for $I_{leakagei}$. However, if the transistor density in the layout varies across the design, as shown for an example layout in Figure 11, then the $I_{leakagei}$ will also vary in each supply pin since the supply rail will distribute the current proportionally as a function of its resistance. The localized variation of the leakage current will adversely affect the localization methods described in the previous section unless it is accounted for.

An observation concerning leakage current is that it is affected most by global variations introduced by changes in process and technology-related parameters. In other words, the current variations introduced by variations in these parameters will affect all transistors and junctions in a device in a similar manner. We are not claiming that intradevice variations do not exist, but rather that they are smaller in magnitude and can be ignored. The more significant global variations will scale the leakage

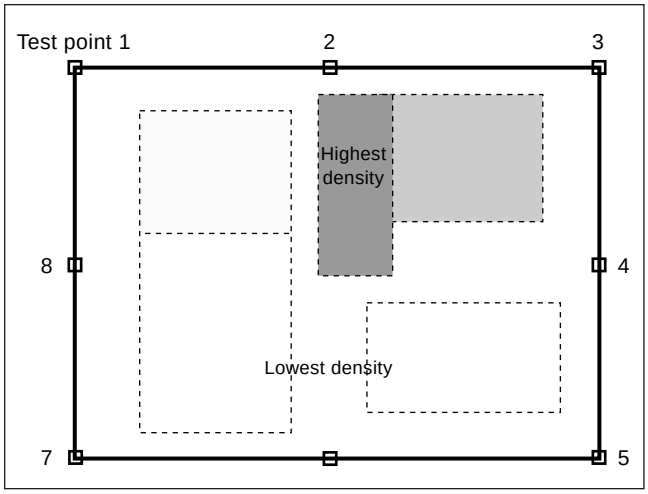

Figure 11. Block-level diagram showing a diversity in transistor density in different areas of a layout.

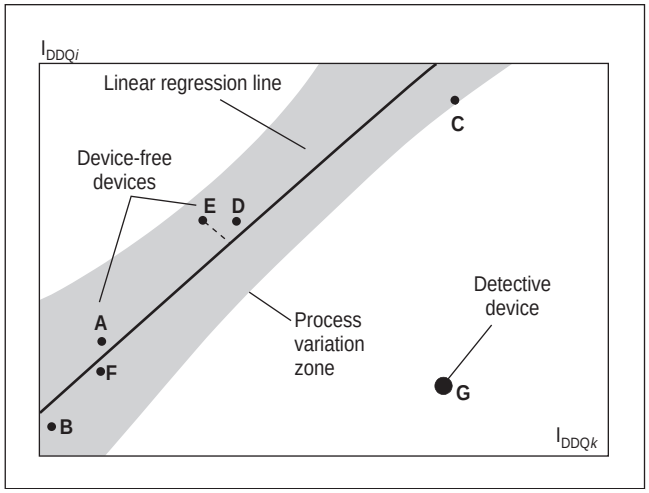

Figure 12. Scatter plot to determine the ratios between each two test points in defect-free devices.

currents in all supply rails proportionally, making it possible to track it using regression analysis.

A graphical representation of leakage current tracking behavior is shown in Figure 12. The x axis plots I_{DDQ} for supply pin *k* while the y axis plots it for supply pin *i*. The labeled points A through F represent measured values on these two pins from a set of defect-free devices. As noted in the figure, the pairs of I_{DDQ} from each device track each other. The regression line (best-fit line) tracks the correlation in these pairings, as shown in the figure. Unmodeled factors such as intradevice process variation and noise will make these data points noncolinear. Therefore, 3 S prediction limits are used to delimit a region around the line (labeled Process Variation Zone). It is within this region that the data points from defect-free devices are expected to fall.

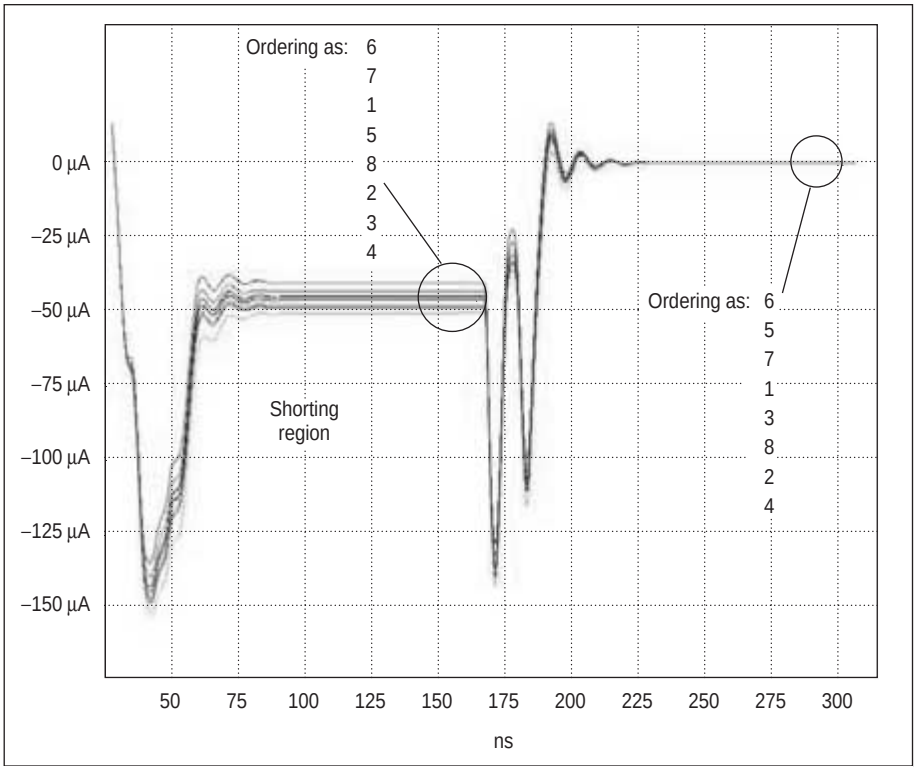

Figure 13. V_{DD} waveforms showing the effects of a shorting defect on the ordering of I_{DDQ} supply pin values.

In contrast, the regional variation caused by an active shorting defect will produce uncorrelated I_{DDQ} in pairings of supply pins. The data point represented by G in the figure shows this for supply pad pairing *k* and *i*. Although we do not present results in this article, defect detection is possible using a strategy based on the analysis of outliers (point G in the figure). The details of such a method are given.[5] Since our focus is diagnostics, only the procedure used to calibrate for process and technology variation effects is outlined here.

Figure 13 illustrates the regional compared to

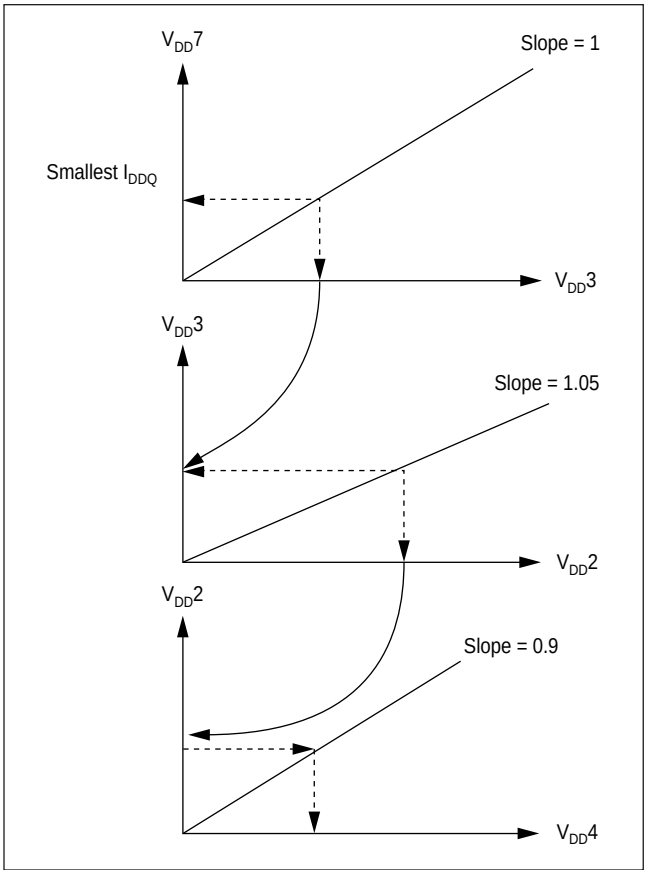

Figure 14. $I_{leakage}$ calibration using backward mapping across scatterplots.

global effect in a set of waveforms. As indicated, the background currents for our experiments are extremely small (< 30nA). However, they are measurable in the noise-free environment of the simulation. The waveforms shown in the figure represent the I_{DDQ} under two different state vectors. The shorting region is the I_{DDQ} under the shorted circuit state (defect activated). The region on the right are the I_{DDQ}s measured under a nonshorting circuit state. Although not discernible in the figure, ordering of I_{DDQ}s under the non-shorting circuit state is different than ordering under the shorting state. Ordering is given in the figure. This is expected since the shorting condition adds different amounts of regional current to the background values depending on the location of the defect with respect to the supply pin. In contrast, the waveforms in either region from a defect-free device are expected to generate the same ordering.

From Equation 4, it is clear that the system of equations is solvable (in the fashion described earlier) if $I_{leakagei}$ are known quantity. There are several alternatives for deriving these values, all of which depend on the existence of a set of scatterplots that correlate the expected I_{DDQ} values between the supply pins of the design. In cases in which the vector-to-vector background current variation remains correlated between the supply pins, the proposed regression analysis for a single state vector can be used across vectors. In this case, an accurate estimate of $I_{leakagei}$ under the shorting circuit state can be obtained from measurements made on the same device under a nonshorting state. A second alternative involves computing the mean value from the set of defect-free characterization devices used to derive the scatterplots. If the vector-to-vector variation is small compared to process variation, then the mean value may be good estimate of $I_{leakagei}$.

The best alternative is a method that accounts for both vector-to-vector and chip-to-chip I_{DDQ} variations. The best way of accomplishing this is to measure the I_{DDQ} of the defective device under the state vector that causes the short, but to do so without causing a short. This is clearly impossible, but a close approximation may be possible. The results presented in Figure 13 give a total ordering of I_{DDQ}s under the shorted circuit state. The largest three current values were selected for the localization methods, and the smaller values were ignored since their supply pins were presumably further removed from the defect site. This suggests that the smallest of these values has the smallest fraction of current drawn by the defect. If it is assumed that this current is entirely leakage current, then this value can be used to derive the leakage components in the other supply pins using the scatterplots derived from defect-free devices.

Figure 14 illustrates this, with three scatterplots showing the relationship of the leakage currents between four supply pads of some design. In this case, I_{DDQ7} is smallest and is used in a backward mapping procedure to obtain the leakage currents for I_{DDQ3}, I_{DDQ2}, and I_{DDQ4}, as shown by the arrows in the figure. Note that slopes other than 1 in the regression lines indicate differences in transistor density across the

layout, as described previously. The $I_{leakagei}$ obtained using this procedure can then be plugged into the equations given in Equation 4 and solved in a manner similar to that proposed for Equation 2.

Conclusion

No other diagnostic method, based on the analysis of electrical signals, has been proposed that is capable of providing physical layout coordinates of defects. This attribute is particularly attractive as top-side die access becomes more difficult and as the number of metal layers increase, making other image-based diagnostic techniques more difficult to apply.

With respect to hardware implementation of the technique, our main concerns relate to instrumentation accuracy. The simulation results of the device in 2.0-micron technology indicate that the ratio between the resistance of the defect network to ground over the equivalent resistances (from the supply pin to the defect site) are on the order of 200 to 1. In other words, a defect that draws 1 mA current will produce I_{DDQ} variations in each supply pin in the 10's of uA range. If the measurement instrumentation is capable of distinguishing between values in that range, then good defect localization accuracy is expected. Technology trends and a better extraction procedure may reduce this ratio in more advanced technologies, further improving accuracy.

Simulations and hardware experiments are under way to investigate other aspects of the QSA procedure. These include experiments designed to test the proposed process calibration techniques. The defect detection capabilities of the method will be evaluated.

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