Characterizing Within-Die Variation from Multiple Supply Port I_{DDQ} Measurements

Kanak Agarwal*, Jim Plusquellic, and Dhruva Acharyya+

*IBM Austin Research Laboratory, University of New Mexico, +Verigy Inc.

Abstract

The importance of within-die process variation and its impact on product yield has increased significantly with scaling. Within-die variation is typically monitored by embedding characterization circuits in product chips. In this work, we propose a minimally-invasive, low-overhead technique for characterizing within-die variation. The proposed technique monitors within-die variation by measuring quiescent (I_{DDQ}) currents at multiple power supply ports during wafer-probe test. We show that the spatially distributed nature of power ports enables spatial observation of process variation. We demonstrate our methodology on an experimental test-chip fabricated in 65-nm technology. The measurement results show that the I_{DDQ} currents drawn by multiple power supply ports correlate very well with the variation trends introduced by state-dependent leakage patterns.

1.0 Introduction

Process variation is typically observed at several different scales such as lot-to-lot, wafer-to-wafer, across wafer and across-field variation. Lot-to-lot and wafer-to-wafer variations are caused by long-term drifts in tools and wafer processing conditions. Across-wafer variation primarily occurs due to wafer-level non-uniformities such as post exposure bake (PEB) temperature gradient [1] and resist thickness variation [2]. Across-field variation, on the other hand, stems from optical sources such as across-field focus and dose variation [3] and mask errors [4]. In addition to the above sources, across-die variation can also be caused by layout dependent systematic effects such as pitch and density dependent line-width variability [5,6] and microscopic etch loading [7].

Different components of variation are routinely monitored in a manufacturing line to predict the health of the line. Large scale variations such as lot-to-lot, wafer-to-wafer, and to a certain extent, across-wafer variation can be adequately monitored by measurements taken from scribe line (physical space between dies allocated for dicing purposes) test structures [8]. These scribe line structures contain a range of test macros required for monitoring different sources and components of variation. However, the scribe-line macros do not provide any coverage of within-die variation. In order to monitor within-die variation, one must place supplemental test circuits on product dies. These structures should be spatially distributed across the 2-dimensional plane of the die to obtain sufficient spatial coverage. This places significant restrictions on the kind, number, and location of the test structures that can be embedded in a chip. This is true because any structure embedded in a product chip should be minimally invasive while adhering to strict design and test limitations such as acceptable power, area, I/O interface, test-cost etc.

There has been a significant body of work in the area of test structure design and process monitoring [9,10,11]. However, due to limitations discussed above, on-product monitors have barely evolved beyond embedded ring oscillators. These ring oscillators are usually placed at multiple locations and their frequencies can be routinely measured to reflect within-die variation. The ring oscillators are usually identical in nature or they can be tuned to cover different circuit styles or heighten their sensitivity to a particular process parameter [12,13]

In this paper, we present a minimally-invasive approach for monitoring within-die variation. Our approach is based on quiescent current (I_{DDQ}) measurements. In the proposed method, individual I_{DDQ} measurements are made at multiple supply ports that are spatially distributed across the area of the chip. The within-die variation profile is extracted from the multiple supply port I_{DDQ} signature. We show that the multiple supply port I_{DDQ} signature, which is a measure of how overall chip I_{DDQ} is distributed across different pads, correlates well with the within-die variation profile. We present experimental hardware data from a test-chip fabricated in 65-nm SOI technology to validate this correlation. We discuss the benefits of the proposed method and argue that it enables a low overhead and minimum perturbation characterization of within-die variability in product chips.

The proposed quiescent current-based method provides several benefits over embedded test structures:

- The method requires only a small on-die test structure to calibrate for resistance variations in the power grid (to be discussed) and therefore, it is minimally invasive. The area and design time overheads of the technique are very small.
- Multiple port I_{DDQ} measurements are made through power supply ports. Therefore, the method leverages the existing architectural component of the chip for data collection whereas embedded structures may require additional ports for measurements.
- Given that the spatial separation between supply ports is typically less than 500 microns in C4-based chips, and many ICs posses hundreds of such power ports, the technique provides a high level of resolution of with-in die leakage variation. The widely distributed nature of the power ports enables a chip-wide or a specific region-based analysis to be carried out.
- The technique requires no more tester time than other embedded test structures, such as the embedded ring oscillator scheme described previously, thereby enabling regular monitoring of within-die variation with minimal test-overhead.
- I_{DDQ} measurements are very robust in characterizing long-range spatial variations. This is true because I_{DDQ} measures the aggregate effect and thus naturally eliminates local random and local layout dependent effects.

The remainder of the paper is organized as follows. In the next section, we discuss the multiple supply port measurement technique and its application in characterizing within-die variation. In Section 3.0, we present hardware measurement results before concluding in Section 4.0.

2.0 Experimental Design and Setup

I_{DDQ} testing is a well known method for defect detection but the efficacy of I_{DDQ} testing has been diminished due to large background static leakage currents in current technologies. The problem is further exacerbated due to exponential dependence of leakage on process parameters such as channel length and threshold voltage. Process variation can cause an order of magnitude variation in chip leakage [14], thereby making it hard to isolate defect current from the leakage variation. However, in the absence of defects, chip-to-chip I_{DDQ} variation is a reliable indicator of die-to-die variation and can be used to extract chip-mean values of process parameters. The chip-wide I_{DDQ} does not contain information to extract within-die variation. A multiple supply port (MSP) measurement technique has previously been proposed for defect testing [15]. In this section, we discuss the MSP measurement technique and show that it can be used to extract across die variation profile from I_{DDQ} measurements1[1].

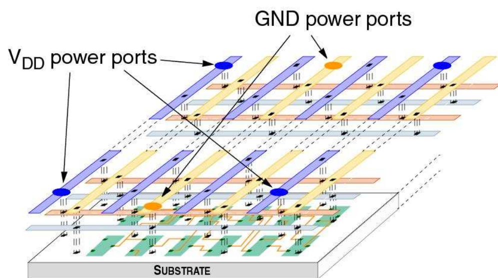

Figure 1. Multi-layer power grid with C4 bumps as power ports. The power ports are distributed across the 2-D plane of the chip.

The power grids of most commercial products interface to an external power supply through multiple power ports. The interface can be through peripheral pads or through a C4 bump array, as shown in Figure 1. The power ports of the latter are distributed across the 2-dimensional plane of the chip to minimize IR and Ldi/dt voltage variations introduced by the finite resistance of the metal that defines the power grid[2]. The distributed nature of the power ports enables regional observation of the current distribution characteristics of the chip. The multiple supply port I_{DDQ} technique measures currents drawn from the individual power ports distributed across the surface of chip. The I_{DDQ} currents drawn from multiple ports reflect the regional composition of the overall chip-wide I_{DDQ}.

Within-die variation is highly spatially correlated [16] and hence it impacts the regional distribution of I_{DDQ} by increasing leakage in the faster regions of a chip while reducing it in the slower regions. Within-die variation, therefore, modulates the I_{DDQ} currents drawn from spatially distributed power supply ports. For a chip with N power ports, we define a MSP I_{DDQ} signature as an N-dimensional vector I_{MSP}, given by Eq. 1: Here, I_1

$$I_{MSP} = [I_1, I_2, \ldots I_N] \qquad \textbf{Eq. 1.}$$

to I_N represent the currents drawn from the N individual power supply ports.

The intuition behind using the MSP I_{DDQ} signature to sense within-die variation is that if a specific region of a chip becomes slow or less leaky, then the MSP I_{DDQ} signature reflects this profile by having a lower relative leakage contribution in the ports supplying current to that region[3]. Similarly, a faster or leaky region alters the MSP I_{DDQ} signature by increasing the leakage contribution of the neighboring ports.

3.0 Experimental Results

We validated the proposed multiple supply port I_{DDQ} method through hardware measurements. The measurements were taken on an experimental test-chip fabricated in 65-nm SOI process. In this section, we present the details of the test-chip and demonstrate the sensitivity of the MSP I_{DDQ} signatures to within-die variation profiles.

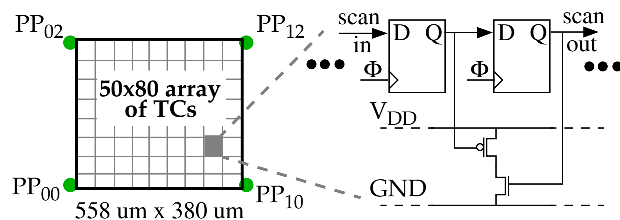

Figure 2. Block diagram of the test macro. The macro contains four power ports labeled as PP_{00}, PP_{02}, PP_{10} and PP_{12}. Schematic of one test-circuit is also shown. The other test circuits are identical.

The block diagram of the test-chip is shown in Figure 2. The test-chip consists of an array of test circuits (TCs) as shown in the figure. There are a total of 4,000 TCs arranged in 80 rows and 50 columns. Each TC in the array comprises of a *pseudo test inverter* with a PFET and an NFET device connected in series between VDD and GND. The gate terminals of the PFET and the NFET devices in the pseudo inverter are independently controlled through scan flops. The scan flops of all TCs are connected in a scan chain configuration. The power to the test array is supplied through four power ports located at four corners of the array and labeled as P_{00}, P_{02}, P_{10} and P_{12} in the figure. Each power port wires out of the chip on a separate pin. The individual current drawn by each of these four power ports can be measured to obtain MSP I_{DDQ} signatures of the test array.

The proposed technique is applied during wafer-probe where it is possible to easily access the individual power ports of the die. The biggest challenge in obtaining accurate measurements during

1. I_{DDQ} is state-dependent. However, this does not impact the usefulness of the proposed technique. The appropriate state in which to place the chip for the most effective characterization of leakage can be determined in advance from simulations.
2. Although a spatial with-in die characterization of leakage is possible for peripheral pad ICs, the resolution of the proposed technique is reduced over that available in C4-based chips because of the pad placement constraints.

3. Relative is defined with respect to the leakage distribution provided by a simulation model with no within-die variations modeled.

wafer probe is dealing with the resistance variations that occur in the power grid, the contactors in the probe card and the external power supply wiring. Resistance variations will introduce changes in the distribution profile of the MSP I_{DDQ} signature that will be indistinguishable from the true I_{DDQ} regional variations that occur on the chip due to within-die variation. In order to eliminate the impact of resistance variations, we use a calibration technique similar to the method proposed in reference [17].

The calibration technique requires the insertion of a low overhead infrastructure on the chip that consists of a distributed array of stimulus-generating circuits, called calibration circuits, similar in design to test circuit shown in Figure 2. One copy of a calibration circuit is placed under each of the power ports. For the power grid under investigation in this work (see Figure 2), we use the TCs under the four power ports as the calibration circuits. A shorting stimulus can be applied to the power grid by enabling both the NFET and PFET devices in the pseudo inverters. The calibration process for a chip involves enabling the calibration circuits, one at a time, and measuring the corresponding shorting currents through each of the power ports. Note that the magnitude of the shorting current created by the calibration circuits is on the order of one mA, so power grid integrity issues are not a concern. A 2-D array of currents is constructed in this fashion, with rows corresponding to the calibration tests and columns corresponding to the power ports. This matrix is used with the data collected from a corresponding set of calibration tests carried out on a simulation model to define a linear transformation operator X. The matrix X is used to calibrate the measured MSP I_{DDQ} signatures, thereby significantly reducing the impact of resistance variations. Details of the procedure are given in reference [17].

We can measure the MSP I_{DDQ} signature of the test macro and extract within-macro variation from the measured data. However, the foot-print of the test macro (558 um x 380 um) is not large enough to observe significant across-macro variation. Hence, in order to validate the correlation between the MSP I_{DDQ} signature and within-die variation, we artificially create different leakage profiles in the macro. The control structure of the test circuit shown in Figure 2 allows us to program leakage currents in different regions of the macro. The leakage of a region can be controlled by varying the input state of the test circuit inverters in the region. If the test inverters in a region are set in the state where both NFET and PFET are off, it emulates the low leakage (and hence higher V_T or higher L_{eff}) region. Similarly, the leakage of a region can be enhanced by setting the test inverters in the region to the input state where either the NFET or PFET is off while the other device is on. Furthermore, by controlling the number of inverters that are in the high or low leakage state in a region, we can arbitrarily program various across-macro leakage patterns.

Figure 3 shows the set of within-die leakage profiles that were artificially created and analyzed in the experiments. Here leakage state 1 corresponds to the low leakage case where both NFET and PFET devices in the test circuit are off and leakage state 2 represents the high leakage state where only the PFET is off while the NFET is on. The leakage patterns shown in Figure 3 exercise the following configurations:

- P0: All test inverters are in the leakage state 2. This state reflects the base state with no within-die variation. The MSP I_{DDQ} signatures of all other patterns are compared against this pattern.
- P1: Alternating test inverters are in leakage states 1 and 2. This state also reflects no within-die variation but a lower global I_{DDQ} than under state P0.
- P2: Alternating test inverters in the lower left quadrant are in leakage states 1 and 2. The inverters in the remaining three quadrants are in the leakage state 1. This state reflects a within-die trend where lower left quadrant is leakier (faster) than the other regions.
- P3: Same as pattern P2 but with all inverters in the lower left quadrant being in the high leakage state 2. This state emulates a scenario where the within-die variation profile is similar to pattern P2 but the magnitude of variation is larger than that in pattern P2.
- P4: Alternating test inverters in the lower half are in leakage states 1 and 2. The inverters in the top half are in the leakage state 1, thereby reflecting an across-die trend where lower half is leakier (faster) than the top half.
- P5: Same as P4 but with all inverters in the lower right quadrant being in the leakage state 2.
- P6: Same as P4 but with all inverters in the lower half being in the leakage state 2.
- P7: Gradient with incrementally larger numbers of inverters per row in leakage state 2. For example, top row has no inverters in leakage state 2, second row has 2 inverters in leakage state 2, ..., bottom row has all inverters in leakage state 2. The pattern creates a downward leakage gradient with the bottom row being leakier than the top row. This pattern may more accurately represent the expected with-in die spatial characteristics in larger chips.
- P8: Same as P7 with direction of increasing leakage upward.
- P9: Same as P7 with direction of increasing leakage to the right.
- P10: Same as P7 with direction of increasing leakage to the left.

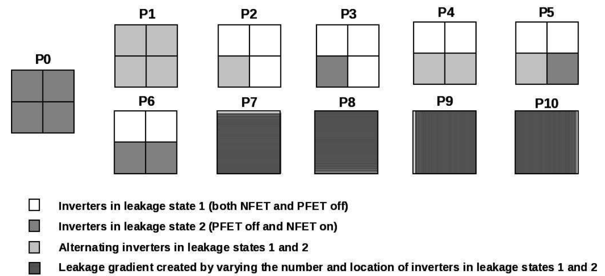

Figure 3. Leakage profiles created in the macro to emulate different within-die variation trends. The leakage profiles were created by controlling the leakage state of the test inverters.

We measured the MSP I_{DDQ} signatures for the eleven leakage patterns discussed above. The relative changes in the I_{DDQ} signatures for patterns P1 to P10 are computed relative the base case, pattern P0. Figure 4 shows the measurement results for one chip. The figure shows the relative change in the current ratio for the four power ports (clusters of 4 bars) under the 10 leakage patterns. The relative change for each PP is calculated as ($I_{pattern}$ - I_{ref})/I_{ref}*100. In other words, the bar heights are computed by

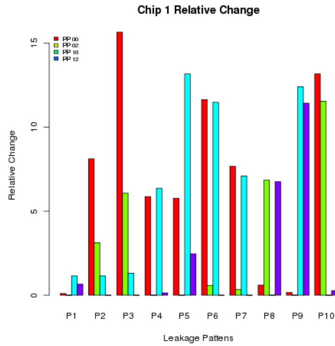

Figure 4. Relative change in MSP I_{DDQ} signatures for different leakage patterns. The change is measured relative to the pattern P0 with no within-die variation.

dividing, port-by-port, the differences in the MSP I_{DDQ} signatures measured under each of the leakage and reference patterns by the MSP I_{DDQ} reference signature and then multiplying each by 100 to express them to a percentage. In order to focus on the I_{DDQ} variations that occur under different leakage patterns, the PP with smallest relative magnitude is subtracted from the other PP currents under that leakage pattern. This effectively removes the DC component. (Therefore, one PP bar in each cluster will be zero.) We refer to this relative change metric as a 'ratio'.

If we compare the results from Figure 4 against the leakage patterns shown in Figure 3, we can see that the two exhibit strong correlation. For example, pattern P1 does not create a within-die variation trend but rather lowers overall global I_{DDQ} (the DC component that is removed) for the chip. Therefore, the change in the PP ratios for pattern P1 over pattern P0 is almost negligible. On the other hand, patterns P2 and P3 make the lower left quadrant leakier than the other three quadrants. This trend is reflected in the increased ratio for PP_{00} (approx. 8% and 16% larger for patterns P2 and P3, respectively), which is in the closest vicinity of the leaky quadrant. The ratios for the PPs on the right side of the grid, i.e., PP_{10} and PP_{12} are similar to the ratios obtained under P0 and P1, as expected. The doubling of the current ratio in PP_{00} nicely reflects the fact that twice as many test inverters are in their high leakage state under P3 as is true for P2.

Similarly, if we look at the measured results for patterns P4 to P6, we see that they all result in an increase in current ratio for ports situated in the lower half of the macro (PP_{00} and PP_{10}). Patterns P4 and P6 exhibit rather symmetric impact on ports PP_{00} and PP_{10} with only a magnitude difference reflecting again the different number of test inverters in the high leakage state. On the other hand, P5 causes a relatively larger change in the PP_{10} ratio than the PP_{00} ratio due to asymmetric nature of the leakage pattern. The correlation between the region of high leakage and the MSP signatures for gradient leakage patterns P7 through P10 is also very strong. These results indicate that the MSP I_{DDQ} ratios not only track the spatial profile of within-die variation, but the magnitude of the change in the MSP I_{DDQ} signature is also proportional to the degree of within-die variation introduced by the leakage patterns.

The above experiments were carried out on ten chips. Figure 5 shows the 'relative change' metric for the chips in box-plot form in a set of four graphs, one graph for each power port. The box-plot depicts the spread of the ratios across the chips for each leakage pattern. Given the small size of the macro and the fact that the ratios are computed relative to the base leakage current on the same chip, it follows that the variances should be very small. Although a portion of the variance is due to intra-die variation, the main source of the variance is measurement noise. This is most evident in the box-plots for leakage patterns P2 and P3 where the majority of the test inverters in the array are configured in their low leakage state and therefore, the magnitude of the current measured for this pattern is closer to the noise floor. We computed the noise floor for patterns P2 and P3 to be approximately 4%, and the noise floor for the other patterns to be in the range of 1-2%. Setting this aside, the figure clearly shows that the programmed within-die patterns modulate the I_{DDQ} signatures in a fairly consistent manner. These results validate our claim that the MSP I_{DDQ} signature is a reliable indicator of within-die variation.

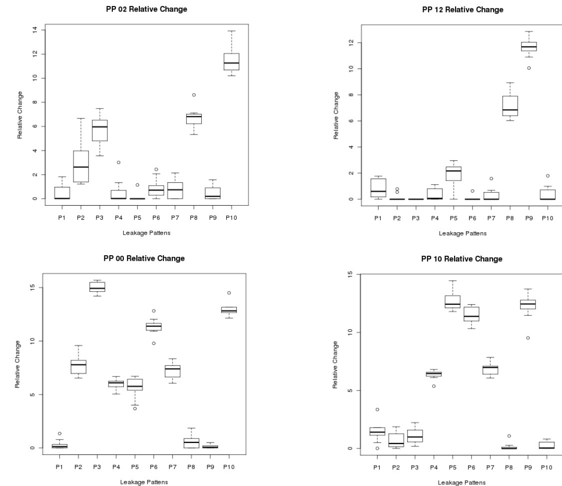

Figure 5. Box-plot of relative change in the I_{DDQ} ratios of four power ports for the leakage patterns in Figure 3.

4.0 Conclusions

We proposed a method for monitoring within-die variation using multiple supply port I_{DDQ} measurements. The proposed method has a small design and test cost and provides a unique capability over other existing characterization techniques. Our results show that the multiple supply port I_{DDQ} signature, which is a measure of how overall chip-wide I_{DDQ} is distributed among various power ports, correlates very well with the within-die variation. To address test cost issues, a practical and realistic measurement strategy is proposed for wafer-level testing that is capable of measuring a large number of power port currents simultaneously. Due to its minimally invasive nature and low-overhead, the proposed technique can enable regular monitoring of within-die variability in product chips.

References

[1] Y. Lee, M. Sung, E. Lee, Y. Sohn, H. Bak and H. Oh, "Temperature Rising Effect of 193nm Chemically Amplified Resist during Post-Exposure Bake", SPIE, vol. 3999, pp. 1000-1008, 2000.

[2] C. Berger et al., "Critical Dimension Variations of I-line Pro-

cesses due to Swing Effects", SPIE, vol. 6153, pp. 61523T, 2006.
[3]Y. Borodovsky, "Impact of Local Partial Coherence Variations on Exposure Tool Performance", SPIE, vol. 2440, pp. 750-770, 1995.
[4]A.K. Wong, R. Ferguson and S. Mansfield, "Mask Error Factor in Optical Lithography", IEEE Trans. on Semi. Manuf., vol. 13, pp. 235-242, May 2000.
[5]D.G. Chesebro et al., "Overview of Gate Linewidth Control in the Manufacture of CMOS Logic Chips", IBM J. of Res. and Dev., vol. 39, pp. 189-200, Jul 1995.
[6]J.-Y. Lai, N. Saka and J.-H. Chun, "Evolution of Copper-Oxide Damascene Structures in Chemical Mechanical Polishing", J. of Electrochem. Soc., pp. G31-G40, 2002.
[7]C. Hedlund, H. Blom and S. Berg, "Microloading Effect in Reactive Ion Etching", J. of Vacuum Science and Tech., vol. 12, pp. 1962-1965, 1994.
[8][C. Hess et al., "Scribe Characterization Vehicle Test Chip for Ultra Fast Product Wafer Yield Monitoring", Intl. Conf. on Microelectronic Test Structures, pp. 110-115, 2006.
[9]K. Agarwal and S. Nassif, "Characterizing Process Variation in Nanometer CMOS", Design Automation Conf., pp. 396-399, 2007.
[10]M. Ketchen and M. Bhushan, "Product-Representative "At Speed Test Structures for CMOS Characterization", IBM J. of Res. and Dev., vol. 50, pp. 451-468, Jul 2006.
[11]D. Boning et al., "Test Structures for Delay Variability", TAU Workshop, pp. 109, 2002.
[12]M. Bhushan, A. Gattiker, M. B. Ketchen and K. K. Das, 'Ring Oscillators for CMOS Process Tuning and Variability Control", IEEE Trans. on Semi. Manuf., vol. 19, pp. 10-18, Feb. 2006.
[13]L. Wang, W. Pope, L-T. Pang, A. Neureuther, E. Alon and B. Nikolic, "Hypersensitive Parameter-Identifying Ring Oscillators for Lithography Process Monitoring", SPIE, pp. 750-770, 2008.
[14]S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi and V. De, "Parameter Variations and Impact on Circuits and Microarchitecture", Design Automation Conf., pp. 338-342, 2003.
[15]C. Patel, E. Staroswiecki, S. Pawar, D. Acharyya and J. Plusquellic, Diagnosis using Quiescent Signal Analysis on a Commercial Power Grid, International Symposium on Testing and Failure Analysis, Nov. 2002, pp. 713-722.
[16]P. Friedberg, Y. Cao, J. Cain, R. Wang, J. Rabaey and C. Spanos, "Modeling Within-Die Spatial Correlation Effects for Process-Design Co-optimization", Intl. Symp. on Quality Elec. Design, pp. 516-521, 2005.
[17]D. Acharyya and J. Plusquellic, “Calibrating Power Supply Signal Measurements for Process and Probe Card Variations”, Defect Based Testing Workshop, April 2004, pp. 23-30.