Comparison of Initial Cell Search Algorithms for W-CDMA Systems Using Cyclic and Comma Free Codes

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Abstract- **In an asynchronous CDMA system the first step when a mobile station is switched on is to perform code and time synchronization with the base station. This process of achieving synchronization with the base station is called initial cell search. The code and time synchronization in the cell search process is divided into three stages: (1) slot boundary detection, (2) code group and frame boundary identification, and (3) scrambling code identification.**
This paper proposes an Improved cell search design which uses cyclic codes (Improved CSD) and compares it to the 3GPP cell search design using comma free codes (3GPP-comma free CSD) in terms of a) hardware specifications on a Xilinx Virtex-E FPGA and b) acquisition time measures for different probabilities of false alarm rates. Our results indicate that for a AWGN channel model in a high signal-to-noise ratio environment the Improved CSD scheme requires fewer slots in stage 2 than the 3GPP-comma free CSD scheme. The Improved CSD scheme thus achieves faster synchronization with the base station. At the same time the Improved CSD has a lower equivalent gate count as compared to the 3GPP-comma free CSD for the same length sequences used in stage 2. Hence, our findings indicate that the Improved CSD is a better design as compared to the 3GPP-comma free CSD.

1.0 Introduction

The mobile station needs to achieve code and time synchronization with the base station before any communication with the base station can start. The process of searching for a cell and achieving synchronization with the base station when the mobile station is switched on is referred to as initial cell search [1][2][3]. Cell search needs to be completed with minimum delay as it impacts the system performance. The process of achieving code and time synchronization in the cell search algorithm is divided into three stages 1) slot boundary detection, 2) code group and frame boundary identification, and 3) scrambling code identification. In an asynchronous W-CDMA system, cells are identified by 512 distinct downlink scrambling codes. The 512 codes are divided into 32 code groups to distinguish different base stations and in each code group there are 16 codes. The number of code groups can however be increased from 32 to 256 [4].

This study proposes an Improved cell search design which uses cyclic codes [5] and compares it to the 3GPP cell search design using comma free codes [2]. The acquisition time and the hardware specifications of both the algorithms are compared. The 3GPP-comma free CSD used in this study improves upon the previous work done by Li *et al.* [6] by using a Fast Hadamard Transformer (FHT) in stage 2 which achieves lower hardware complexity and faster decoding.

Furthermore, use of masking functions in stage 3 of both the Improved CSD and the 3GPP-comma free CSD reduces the number of scrambling code generators required in Li *et al's* design. This results in a reduction in the ROM size required to store the initial phases for the scrambling code generators in stage 3. The Improved CSD proposed in this study aims to achieve faster synchronization between the mobile station and the base station.

2.0 Cell Search Procedure

Figure 1 shows the slot and frame structure of the three synchronization channels used in cell search: the Primary Synchronization Channel (P-SCH), Secondary Synchronization channel (S-SCH) and the Common Pilot Channel (CPICH). Each frame of 38400 chips is divided into 15 slots. Each slot is of 2560 chips. In the P-SCH, a 256 chip sequence is transmitted at the start of each slot. The same P-SCH sequence is used by all the base stations and is transmitted once every slot. The S-SCH is used for carrying 15 different sequences one in each slot for the different code groups and is repeated after every frame. From the code group and the slot identification the frame boundary can be detected. The CPICH is used to carry the downlink common pilot symbols scrambled by the scrambling code of the base station. Each slot of this channel is divided into 10 symbols each of 256 chips.

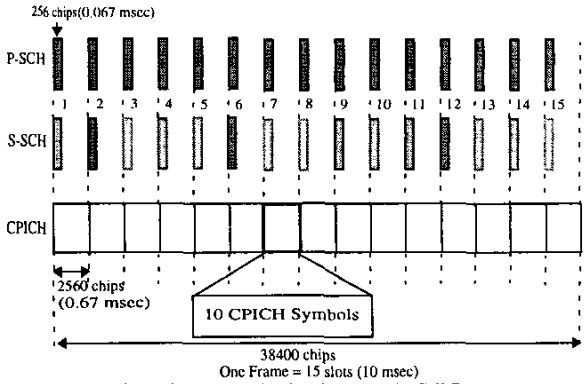

Figure 1: Synchronization Channels in Cell Search

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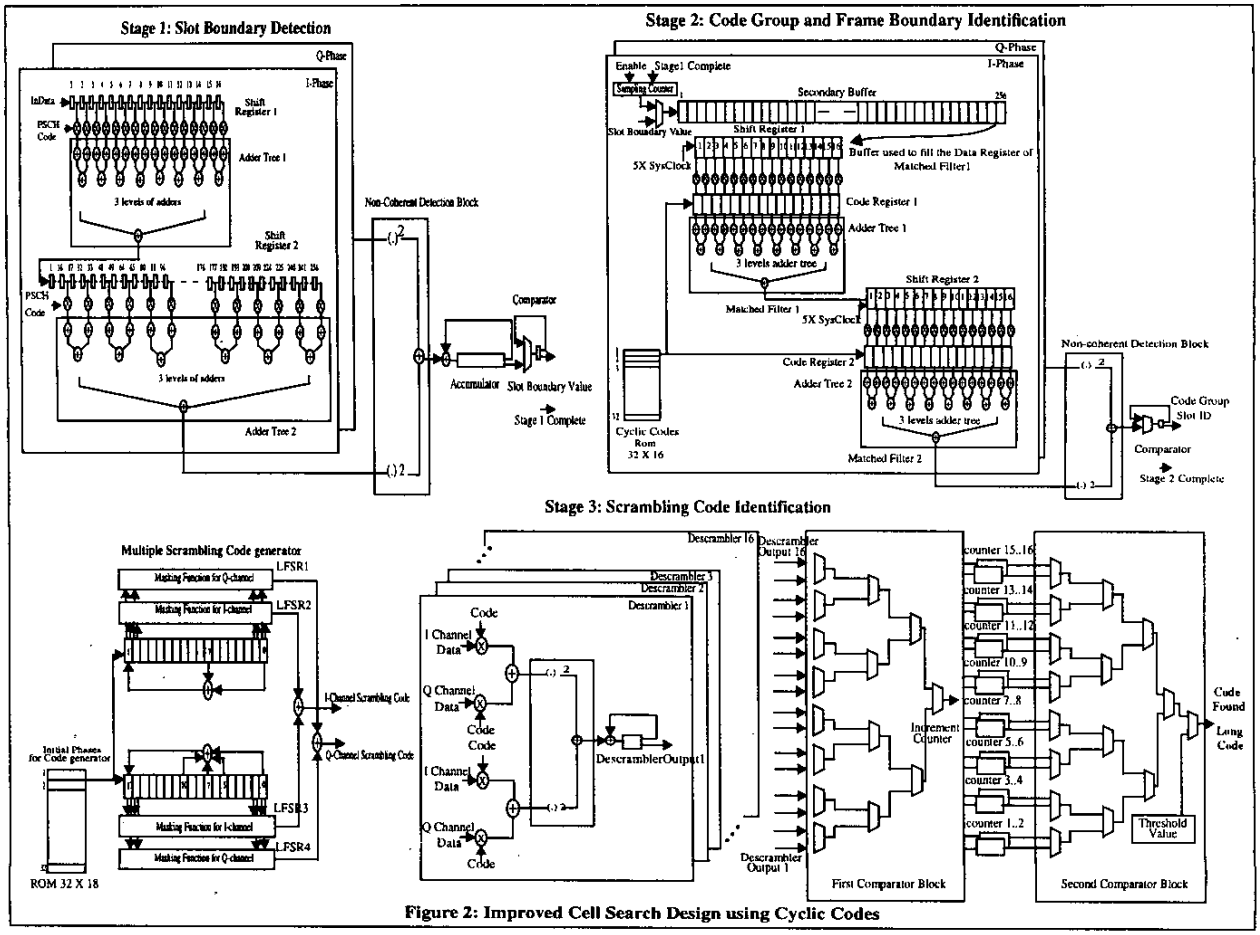

Figure 2: Improved Cell Search Design using Cyclic Codes

3.0 Experimental Design

Improved Cell Search Design using Cyclic Codes (Improved CSD)

Figure 2 presents the system view architecture of the Improved CSD. Stage 1 in the cell search scheme is responsible for identifying the slot boundary. The scheme employed in the Improved CSD is to accumulate energies using data over multiple slots. Experiments were carried out using data over 2, 4, 8 and 15 slots. It was found through experiments that accumulation over 15 slots is sufficient to correctly detect the slot boundary values. The maximum of the accumulated energies obtained after correlating data over 15 slots (38400 chips) is the slot boundary. This slot boundary corresponds to the base station which is closest to the mobile station and the mobile needs to synchronize with this base station. The slot boundary value is then assigned to stage 2.

Stage 2 is responsible for detecting the code group and slot ID of the base station. The frame boundary identified from the slot ID is used to achieve time synchronization with the base station. In this stage no accumulation over multiple slots is needed since the code group and slot ID can be identified using data over 1 Synchronization Channel (SCH) sequence which consists of 256 chips. In the Improved CSD scheme two clocks are used, a slow clock called the system clock in the design and a fast clock which runs at 5X system clock. Two clocks are needed so that the code group and slot ID can be identified before data for the next slot comes in. Thus the Improved CSD scheme takes advantage of the fact that processing for stage 2 is already done before the next data bits come in. The Improved CSD also uses a smaller size ROM 32X16 to store the cyclic codes as compared to the 3GPP-comma free CSD which uses a ROM of size 32X60 to store the comma free codes.

In stage 3, 16 scrambling codes need to be generated in parallel. This can be done with 16 code generators. However, generating the codes in parallel using 16 code generators could be expensive as a huge ROM would be required to store the initial phases for all the 16 code generators. In the Improved CSD only *one* scrambling code generator is used to generate 16 codes in parallel when 32 code groups are used. Sixteen masking functions are used to generate the codes in parallel [7]. Masking functions generate codes which have minimum overlap and also reduce the hardware

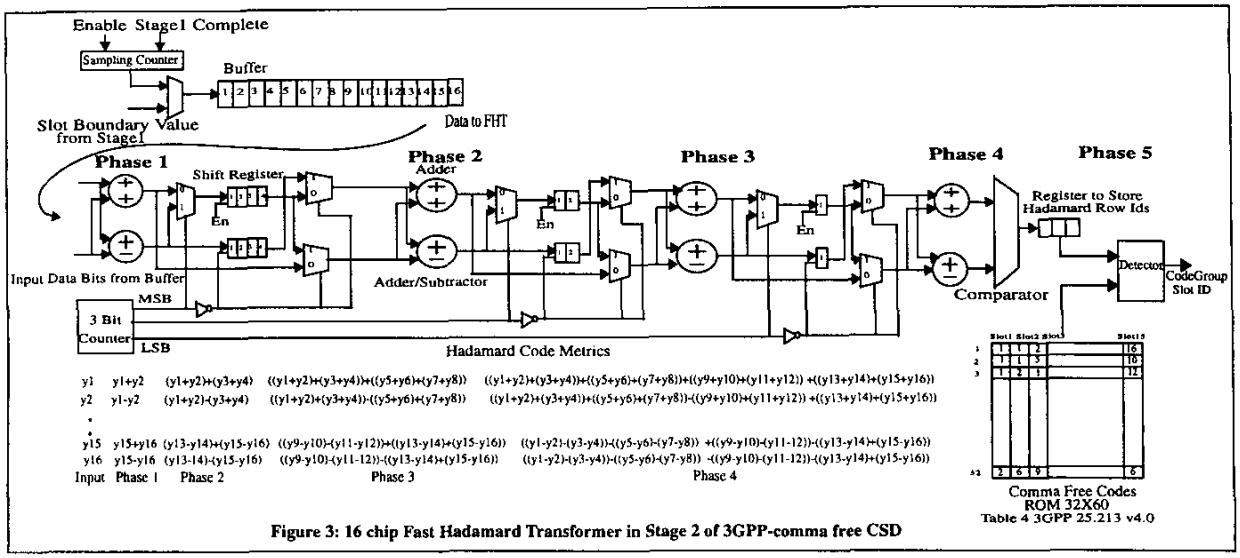

Figure 3: 16 chip Fast Hadamard Transformer in Stage 2 of 3GPP-comma free CSD

circuitry to a single scrambling code generator. The use of masking functions leads to savings in hardware resources at the expense of a few logic gates. Any masking function can be selected by the designer but it should generate codes which have minimum overlap. Besides reducing the hardware from 16 code generators to one code generator, the design also reduces ROM size to 32X18 as compared to 512X18 if 16 code generators were used. Counters are used as shown in Figure 2 Stage 3 to keep track of the votes obtained after the descrambling and the comparison operations. After these operations are completed, the final step is to decide whether cell search has been successful and a code has been found. For this purpose a parameter called probability of false alarm rate is used to predefine the threshold value. If the counter exceeds the predefined threshold value then the cell search operation is declared a success and the particular long code is identified.

3GPP Cell Search Design using Comma Free Codes (3GPP-comma free CSD)

Figure 3 shows stage 2 of the 3GPP-comma free CSD using comma free codes. Stage 1 and stage 3 for the 3GPP-comma free CSD design were kept the same to compare stage 2 of both the designs. The table provided in the 3GPP Specifications [2] for the comma free codes is for 64 code groups. For comparison with the Improved CSD scheme which uses 32 code groups only 32 of the possible 64 code groups are used. Each number in this table is related to a Hadamard row. Accumulation over at least three slots is necessary to uniquely identify a code group in this design. These correspond to the three rows of the Hadamard matrix. A Fast Hadamard Transformer (FHT) is used for detecting code sequences in stage 2. The FHT reduces the hardware required for this stage. If the 256 chip sequences of the Hadamard matrix are observed carefully then it is noticed that the 256 chip sequences can be reduced to 16 chip sequences. Since there are 16 possible sequences this design can be reduced from decoding 16X256 chip sequences to 16X16 chip sequences. Once the three Hadamard rows are identified then it is the job of the detector to find which of the code group is being used from the table. The metrics for the FHT are generated using the butterfly operation which is also used for other DSP applications such as FFT. The butterfly operation involves only addition and subtraction and no multiplier is needed. A 3-bit counter is used for selecting the phases as shown in Figure 3. Use of a counter to select each of the phases of the FHT leads to a reduction in hardware resources required for implementation. Once the metrics are generated then the largest metric is selected the winner and is identified as the possible Hadamard row. The same process repeats for data collected from two more slots to completely detect the code group.

The detector needs to identify the code group in the minimum amount of time which uses a lot of hardware resources. Also if the correct sequence of Hadamard rows is not identified and given to the detector then it can lead to wastage of additional clock cycles as it will try to find the sequence from the table provided in the 3GPP Specifications [2]. The detection circuitry is used to locate the sequence from the table and hence find the code group and slot ID. Also, in the 3GPP-comma free CSD implementation two clocks are not needed. Even if two clocks are used no gain will be achieved as the decoding cannot start till at least three slots have been identified.

4.0 Experimental Method

To compare the acquisition time between the Improved CSD and the 3GPP-comma free CSD, experiments were

Table 1: Hardware Specifications of System: Quantization 4 Input Data Bits, 256 chip Sequence in Stage 2

FPGA XCV 1000E BG560 Speed Grade 6	Number of Slice Registers	Number of 4 Input LUTs	Equivalent Gate Count	Max. Frequency of Operation (Post Route Timing)
Improved CSD	9086	7354	136297	22.066 MHz
3GPP-comma free CSD	10141	7777	144180	12.887 MHz

carried out for two different probabilities of false alarm rates ($P_{FA}=10^{-3}$ and $P_{FA}=10^{-4}$). Threshold values were computed for each alarm rate using the following equation $P_{FA}=e^{-Threshold/V}$, where V is twice the variance of the I and Q components of the AWGN noise [8]. The number of clock cycles between the start of the system and the point when the counter in stage 3 exceeds the computed threshold values was determined. The number of clock cycles gives the acquisition time for both the designs. The equivalent gate count and maximum frequency of operation were compared for both the designs using a 256 chip sequence in stage 2 and same design constraints in the FPGA Express synthesis tool on a Xilinx Virtex-E FPGA XCV 1000E.

5.0 Experimental Results

The threshold values determined for the two false alarm rates ($P_{FA}=10^{-3}$ and $P_{FA}=10^{-4}$) were 28 and 37 respectively. The Improved CSD had a shorter acquisition time as compared to the 3GPP-comma free CSD as observed from Figures 4 and 5.

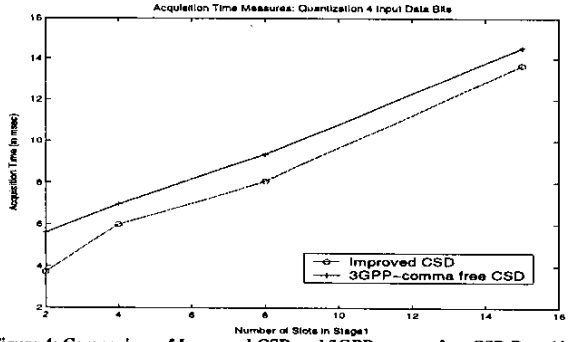

Figure 4: Comparison of Improved CSD and 3GPP-comma free CSD $P_{FA}=10^{-3}$

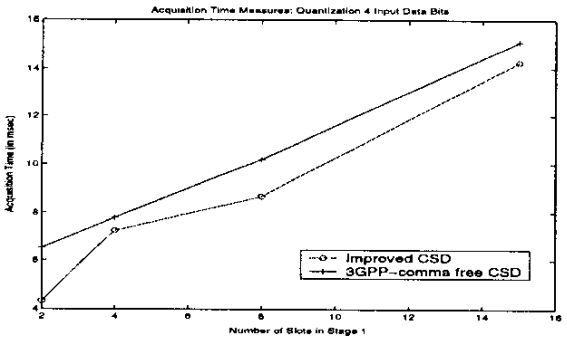

Figure 5: Comparison of Improved CSD and 3GPP-comma free CSD $P_{FA}=10^{-4}$

From Table 1 it is seen that the Improved CSD has a lower equivalent gate count and a higher maximum frequency of operation as compared to the 3GPP-comma free CSD.

6.0 Conclusion

For a AWGN channel model in a high signal-to-noise ratio environment it was found that accumulation over 1 slot in the Improved CSD scheme and accumulation over three slots in the 3GPP-comma free CSD scheme gives correct code group and slot boundary identification. Due to the reduction in the required number of slots in stage 2, the Improved CSD uses lesser number of clock cycles in this stage as compared to the 3GPP-comma free CSD to detect the code group and slot ID. The use of cyclic codes in the Improved CSD has a lower equivalent gate count and a higher maximum frequency of operation as compared to the 3GPP-comma free CSD. In conclusion, the Improved CSD is a better design as compared to the 3GPP-comma free CSD since it has a faster acquisition time and lower hardware utilization.

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