Detection of CMOS Defects Under Variable Processing Conditions

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Abstract

Transient Signal Analysis is a digital device testing method that is based on the analysis of voltage transients at multiple test points. In this paper, the power supply transient signals from simulation experiments on an 8-bit multiplier are analyzed at multiple test points in both the time and frequency domain. Linear regression analysis is used to separate and identify the signal variations introduced by defects and those introduced by process variation. Defects were introduced into the simulation model by adding material (shorts) or removing material (opens) from the layout. 246 circuit models were created and 1440 simulations performed on defect-free, bridging defective and open defective circuits in which process variation was modeled by varying circuit and transistor parameters within a range of +/- 25% of the nominal parameters. The results of the analysis show that it is possible to distinguish between defect-free and defective devices with injected process variation.

1.0 Introduction

Transient Signal Analysis (TSA) is a parametric approach to testing digital integrated circuits [1]. In TSA, defect detection is accomplished by analyzing the transient signals measured at multiple test points of a device. The approach offers two distinct advantages over other logic and parametric testing methods. First, device coupling mechanisms (i.e. power supply) permit the detection of defects at test points that are not directly affected by the defect. Consequently, error observability is greatly enhanced in TSA since they need not be propagated to primary outputs. Second, by cross-correlating the data sampled from multiple test points, false detects caused by mistaking signal variations resulting from process variation as signal variations resulting from defects, are reduced. In fact, all useful parametric test methods must address this problem. The proposed technique works because the effects of process variation tend to be global, changing circuit parameters uniformly across the entire die. Hence, the corresponding change in the transient response of the device produces signal variations that are correlated at all test points on the die. In contrast, signal variations caused by a defect tend to be regional with larger amplitudes at test points closer to the defect site. This results in a change in the cross-correlation profile of the device. A simple statistical method is presented that detects the absence of correlation in one or more test point signals of defective devices while attenuating the signal variations that are correlated or caused by process variation.

In previous work, simulation experiments were conducted on defect-free simulation models with injected process variation and a single 'faulted' simulation model [2][3]. One set of defect-free simulations (calibration simulations) was used to derive the prediction bands while a second set (control simulations) was used to evaluate the accuracy of limits. The detection of the defect using the faulted model was determined using these limits. In this work, the detection of the defect under a **set** of faulted models with injected process variation is determined. In other words, similar to the defect-free simulation experiments, the faulted simulations were repeated using a set of models that were altered by the effects of process variation. Other analysis of the data are presented for completeness of the work and include:

- An analysis of selected subsets of test signals.
- An alternative self-reference signal processing method.
- An analysis of the slopes of the regression lines used to characterize the defect-free devices.

The rest of this paper is organized as follows. Section 2.0 outlines some related work. Section 3.0 describes the TSA method. Section 4.0 presents the experimental setup. Section 5.0 presents experimental results and, finally, Section 6.0 summarizes our conclusions and areas for future investigation.

2.0 Background

Parametric device testing strategies are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of quiescent supply current or transient response. Many types of parametric tests have been proposed but recent research interest has focused on I_{DDT}-based methods.

I_{DDT}-based approaches are designed to overcome the limitations caused by the static nature of the I_{DDQ} test [4][5][6][7]. In general, these I_{DDT}-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as I_{DDQ}, however they do not provide a means of accounting for process tolerances and are therefore subject to yield loss.

Recent related works show promising results and are

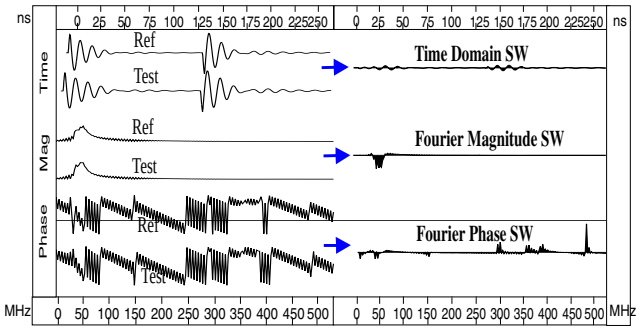

Figure 1. Time and Frequency Domain Signature Waveforms.

based in principle technique that we have proposed [3] and [5]. However, calibration is performed in these techniques across test sequences rather than within a single test sequence. Although these methods are simpler to implement since only one waveform is analyzed per test sequence, it has yet to be determined which of these methods can be adapted to provide adequate defect sensitivities for large deep submicron devices. The multiple test point measurements taken in TSA enhances defect sensitivity at the expense of increased measurement and computational complexity.

3.0 TSA Method and Model

TSA identifies defective devices by cross-correlating the waveforms measured simultaneously at topologically distinct locations on the device as a test sequence is applied to the primary inputs. The power supply, internodal coupling capacitances, well coupling and substrate coupling create an RC network in a digital device which are the mechanisms by which signal variations at a logic node (e.g. due to the presence of a defect) induce signal variations at test points on the power supply. These variations are regional since the RC network attenuates them as the distance from the defective node increases. Therefore, the signals measured at multiple test points can be cross-correlated to detect a defect by analyzing the differences in signal magnitude and phase at the test points. However, signal variations also result from changes in fabrication process parameters, making it difficult to isolate the variations caused by defects. Thus, an important issue is to differentiate between variations due to defects versus those due to process variation. The inability to do so can result in yield loss and test escapes. In previous work, we determined that signal variations caused by changes in the process tend to be global and measurable in all test point signals [1]. More importantly, the signal variations caused by process are proportional across the test points, making it possible to attenuate them using simple signal post-processing techniques. The cross-correlation technique described below is able to calibrate for variations caused by the process and significantly improve the defect sensitivity of the method.

3.1 Signature Waveforms

TSA is based on the analysis of signal differences between a defect-free reference device and a test device. Signature Waveforms (SWs) capture these differences. SWs are created by subtracting the waveform measured from some test point on the test device from the waveform measured from the same test point location on the reference device. An example is shown in Figure 2 in the time and frequency domains. The V_{DD} waveform from the reference (Ref) is shown along the left plot while the V_{DD} waveform from a test device (Test) is shown below it. Subtracting the test waveform from the reference creates a Time or Frequency Domain Signature Waveform shown along the right of Figure 2. The SW is shown shaded to a zero baseline. The area under the curve, computed by evaluating the integral of the waveform using the trapezoidal rule formula over the time interval 0-250ns or frequency interval 0-200 MHz, is referred to as the Signature Waveform Area (SWA).

3.2 Linear Regression Analysis

Linear regression is used to decide the pass/fail status of a test device. Using a set of SWs from simulations, Figures 2 and 3 illustrate TSA. Figure 2 shows two columns of SWs from two test points (Vdd_2 and Vdd_7). The pairs of SWs in the top 6 rows correspond to different simulation experiments designed to model simple changes in the process. In these simulations, exactly one of either *beta* or *vto* was varied globally from the nominal value by the amount shown in the figure. The last row shows the SWs from a simulation conducted on the reference model with a bridging defect inserted.

The SW pairs in the first 6 rows are correlated. In other words, the magnitude of the variations in the SWs of one row is proportional to corresponding SWs in other rows. The SWAs shown on the far right and far left in the figure preserve this correlation. For example, the SWAs for Vdd_2 and Vdd_7 in Defect-Free simulation A are 0.11 and 0.22, respectively, which are proportional to the values 0.04 and 0.08 in Defect-Free simulation B. The Scatter Plot in Figure 3 plots the SWAs of Vdd_2 (x-axis) against the SWAs of Vdd_7 (y-axis) and illustrates that the SWAs from simulations A through F track linearly. Thus, a least squares estimate of a linear regression line (best fit line) shown in the figure tracks process variation in data points A through F. The shaded region around the regression line is called the Process Variation Zone and is delimited by prediction limits. The regression line accommodates good devices in all regions between the process specification corners while the prediction limits account for small non-linearity, measurement noise and intra-device process variations.

In contrast, the SWs labeled G shown along the bottom of Figure 2 are not proportional to the SWs in the other

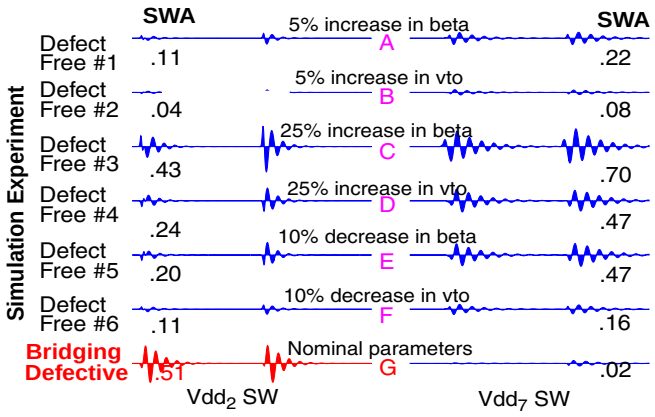

Figure 2. Vdd_2 and Vdd_7 Signature Waveforms from 7 simulation runs.

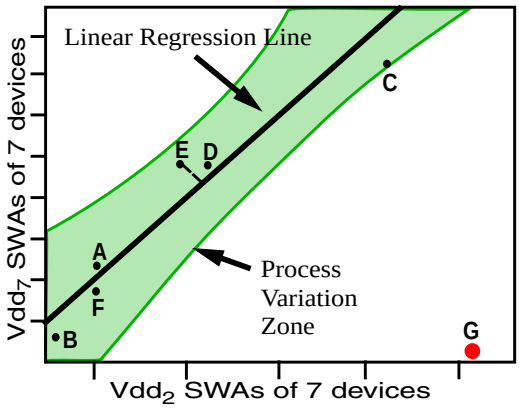

Figure 3. Scatter plot, regression line and prediction limits using data from Figure 2.

rows. In this case, the defect has produced regional variation in the SW of Vdd_2 due to its proximity to this supply rail. A much smaller amount of variation occurs in Vdd_7 due to the attenuation effect of the RC network. The lack of correlation in this pairing is illustrated by the outlier data point G in Figure 3. From the plot, it is clear that the behavior of this device is not characteristic to the norm defined by the prediction limits of the Defect-Free simulations.

3.3 The Pass/Fail Criterion

Based on this example, the pass/fail criterion under each test sequence is straightforward. Across all pairings of test points, if a test device generates a data point that falls outside of the Process Variation Zone for **any** pairing, the test device is defective. However, it may not be necessary to analyze **all** test point pairings to determine this. In this paper, it is shown that one particular subset of test point pairings is sufficient to detect all the defects.

$$y = b_0 + b_1 x \pm W\sqrt{MSE}\sqrt{1 + \frac{1}{n} + \frac{(x-\bar{x})^2}{\sum_i (x_i - \bar{x})^2}} \quad (1)$$

where $W = \sqrt{2F(1-\alpha);2;(n-2)}$

$$\sqrt{MSE} = \sqrt{\frac{\sum (Y_i - \hat{Y}_i)}{n-2}}$$

The pass/fail criterion is based on an analysis of “residuals”. A residual is defined as the shortest distance from the data point to the regression line, as shown in bold in Figure 4. In this figure, a scatter plot of data points from 86 simulations are shown. 48 defect-free simulations (43 calibration and 5 control) were run under different process models and used to derive the regression line and prediction limits. Similarly, 48 “faulted” simulations were also performed to evaluate these limits under variable processing conditions. The 6σ prediction limits are labeled in the plots and defined by Equation (1).

The prediction limits are sensitive to both the number of simulations or samples (1/n in the equation) and the amount of dispersion of the data points around the regression line (Mean Square Error or MSE). For this experiment, the 3σ limits bound the 43 data points used to derive the limits (as expected) but several of the control device data points fall outside of these limits. As explained in more detail in Section 4.1, wider limits (6σ) are necessary to bound the dispersion of control data points for this experiment because the parameters to the model used to derive them were varied in such a way as to approximate worst case process variation.

For the experiments in this paper, the prediction bands are used as the pass/fail threshold for the Test devices (both Control and Faulted). In other words, a test device fails if, in the scatter plot of any test point pairing, at least one residual is larger than the region defined by the prediction limits for that scatter plot.

4.0 Experiment Setup

The experiments were conducted on a full-custom design of an 8-bit 2’s complement multiplier. A block diagram of this device is shown in Figure 5. The power supplies for the core logic are labeled as V_{DD1} through V_{DD10} and are joined internally through a series connection of 2 Ω resistors (shown on the right in the figure) to simulate the supply grid configuration of a larger device. The transients were measured from the Metal2 core logic test pads (overglass cuts shown on the left in the figure), which is representative of conducting TSA at wafer probe. The input test sequences were run at 4 MHz for a duration of 250ns.

The regularity in the structure of the design made it possible to introduce defects at multiple locations while maintaining the ability to easily generate vector pairs which individually targeted a unique defect. The approximate locations of the defects are shown as ‘X’s in Figure 5. Three versions of the multiplier were designed: a defect-

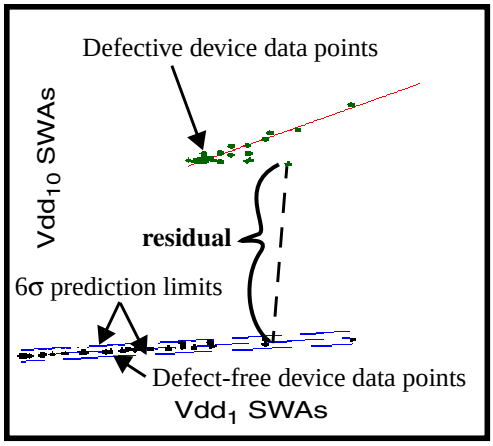

Figure 4. Scatter plot of data points from 86 simulations.

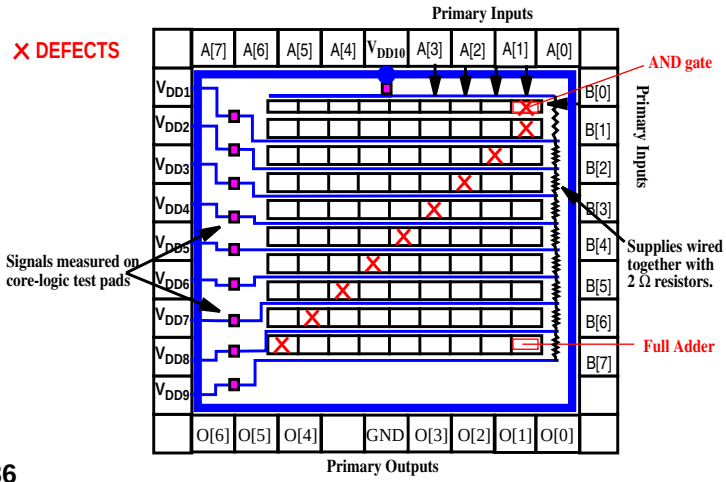

Figure 5. Block-level diagram of the multiplier showing defect locations.

free version, a version with 9 inserted shorts and a version with 9 inserted open defects. The resistance of the shorting defects in the bridging defective circuit varies between 0 Ω (hard short) and 10 KΩ. For the open defective multiplier, the range is 100 MΩ (hard open) and 2 KΩ.

4.1 Experiment Description

Accurate circuit models were generated using the SPACE extraction tool [10]. The lot averaged circuit parameters reported by MOSIS for hardware devices fabricated at 2μ were used to derive the technology file used by SPACE. 18 bridging and open experiments were conducted, each dedicated to detecting exactly one of the 9 bridging or open defects.

A simulation run was made using a nominal defect-free simulation model and either a bridging or open defective simulation model for each of the 18 experiments. In addition, 228 simulation models were extracted from the layout and used to analyze the effects of process variation. In these models, one or more of the transistor and/or circuit parameters reported by MOSIS were varied over the range -25% and +25% of the nominal value.

Table 1 summarizes the simulation experiment models and runs. For example, in Bridging and Open Experiments 1-3 (column 3), models were extracted and simulated in which the parameters shown were changed individually for 30 models, and in groups of nine for 5 models by plus and minus 5%, 10% and 25% of the nominal values. Two additional simulations (Min and Max) were conducted for each of these experiments in which the nine process parameters were all set to -25% and +25% respectively to approximate the worst case process model.

The reference simulations identified in column 2 of Table 1 were used to create the Signature Waveforms as described in Section 3.1. The remaining simulations were divided into two groups, a Calibration group (columns 3 through 5) and a Test group (columns 6 through 8). The Calibration group was used to derive the regression lines and prediction intervals. The Test group was used to evaluate the prediction limits and the defect sensitivity of the method and are further divided into a Control group (column 6) and a Faulted group (columns 7 and 8).

The Control experiments are defect-free simulations designed to approximate extreme cases of process variation and are used primarily to set the prediction limits for each of the three experiment groups. The limits were set such that *no* control data point fell outside of the prediction band. Since the number of simulations varied in the Training group across each of the experiment groups, 1-3, 4-6 and 7-9, it became necessary to set the σ value differently for each of these groups in order to keep the data points in the Control group bound within the prediction bands. The limits were set at 6σ, 8σ and 3σ for the three groups, respectively, to account for training set sizes of 37, 43 and 22 as shown in Table 1. Moreover, a different set of Control experiments were used for each of these experiment groups. The diversity in each of these groups also affected the appropriate σ value and emphasizes the necessity of choosing a training set that characterizes the expected range of process variation.

The second set of simulations in the Test group (columns 7 and 8) were run for each experiment using a model with a defect inserted. Column 7 lists the simulations performed under each of the two faulted simulation models using the nominal circuit parameters. Column 8 lists the simulations performed under each of the faulted simulation models with the process parameters varied as shown in columns 3 through 6. In other words, the defect-free simulation experiments modeling process variation were repeated using each of the faulted simulation models.

5.0 Experimental Results

5.1 Nominal-Reference Analysis

The histograms of Figure 6 show the resulting number

Table 1: Summary of the Simulation Experiments and Models.

	Reference Model	Defect-free Process Model. Calibration	Defect-free Process Model. Calibration	Defect-free Process Model. Calibration	Defect-free Control. Test	Defective Reference. Test	Defective Process Model. Test
Experiments	Br&Op1-9	Br&Op 1-3	Br&Op 4-6	Br&Op 7-9	Br&Op 1-9	Br&Op 1-9	Br&Op 1-9
# of models	1	37	43	22	5	2	162
Total # of sims	18	222	258	132	90	18	702
Transistor/Circuit parameters varied by +/– 5%, 10% and 25%	None	Beta, V_t, poly Ω, metal2 contact Ω, metal cap. over p-/n-well	Beta, V_t, p-/n-diff Ω, metal1 contact Ω, poly cap. to substrate, metal1 to metal2 cap.	All 9 parameters listed to the left.	All 9 parameters listed to the left.	None	Same as columns 3-6
# of circuit parameters varied per model.	None	1 (30 models). 9 (5 models). 9 at Min/Max (2 models).	1 (36 models). 9 (5 models). 9 at Min/Max (2 models).	9 (20 models). 9 at Min/Max (2 models).	9 (15 models).	None	Same as columns 3-6

of "faulted" simulation data points which exceed the prediction limits for each of the 18 simulation experiments. For each experiment, transient data was measured on each of the 10 supply rails simultaneously at the test points shown in Figure 5. Therefore, n*(n-1)/2 or 45 test point pairings are available for analysis under each experiment. The hatched bars in the histograms give the number of data points (out of a possible 45) that fell outside of the prediction limits while the solid bars give the number of outlying data points for a subset of these pairings: the 9 test point pairings involving adjacent Vdds, e.g. Vdd_1-Vdd_2, Vdd_2-Vdd_3, Vdd_3-Vdd_4, etc.

The topmost histogram shows the results for the Time Domain analysis while the middle and bottom histograms show the results for the frequency domain (Fourier Magnitude and Fourier Phase). As indicated in the right-most column of Table 1, various types of process variation were introduced into the faulted models and the experiments were repeated under each of the test sequences. However, the histogram shows the number of outliers obtained from a single faulted simulation run for each experiment. The simulation result reported is the run that produced the minimum number of outliers across all three domains (the worst case).

As indicated in Section 3.2, a defect is detected if at least one data point falls outside of the prediction limits. The results shown in Figure 6 indicate that all defects are detected in one or more domains using either 9 or 45 test point pairings. Since the complexity of the test is, in part, based on the number of pairings analyzed, these results indicate that only a subset of the pairings may be sufficient. The magnitude analysis provides the best results (all defects detected using either 9 or 45 pairings) while the phase analysis yields the worst result (fails to detect 8 defects using 45 pairings and 13 defects using the subset of 9 pairings).

5.2 Self-Reference Analysis

The histograms shown in Figure 6 are labeled Nominal-Reference to indicate that a defect-free reference device model (golden device) was used to create the Signature Waveforms, as explained in Section 3.1. Figure 7 shows a set of histograms obtained from the same data set but using a different Signature Waveform creation procedure. Instead of using a defect-free reference device to create the Signature Waveforms, the waveform from Vdd_1 on each device was used as the reference. Therefore, 9 fewer pairing are available for analysis (36 instead of 45) and one additional sample is available (the defect-free nominal reference simulation). The notion here is to determine if the effects of process variation can be reduced further. The analysis of the scatter plots (not shown) indicates that this is the case.

Once again, all defects are detected in one or more domains. It is also apparent that the Phase results have improved dramatically over the Nominal-Reference results while the Time and Magnitude have changed only marginally. The most straightforward method of comparison is to count the **number of experiments** that have zero outliers in each domain (where lower values indicates a better result). For the Nominal-Reference Time Domain analysis, 5 experiments show zero outliers in the 45 pairing analysis. For the Self-Reference analysis, this value is 3. The Magnitude analysis yields 0 and 1 while the Phase analysis yields 8 and 0, respectively. Ongoing research is investigating the large number of zero outlier experiments (test escapes) in the Phase Nominal-Reference results. This result contradicts the Self-Reference results and the results of previous hardware experiments [2][3].

5.3 Test Point Pairing Analysis and the Vdd_{10} Supply Rail Topology

Other subsets of 9 test point pairings were analyzed. These included pairings involving Vdd_1, e.g. Vdd_1-Vdd_2,

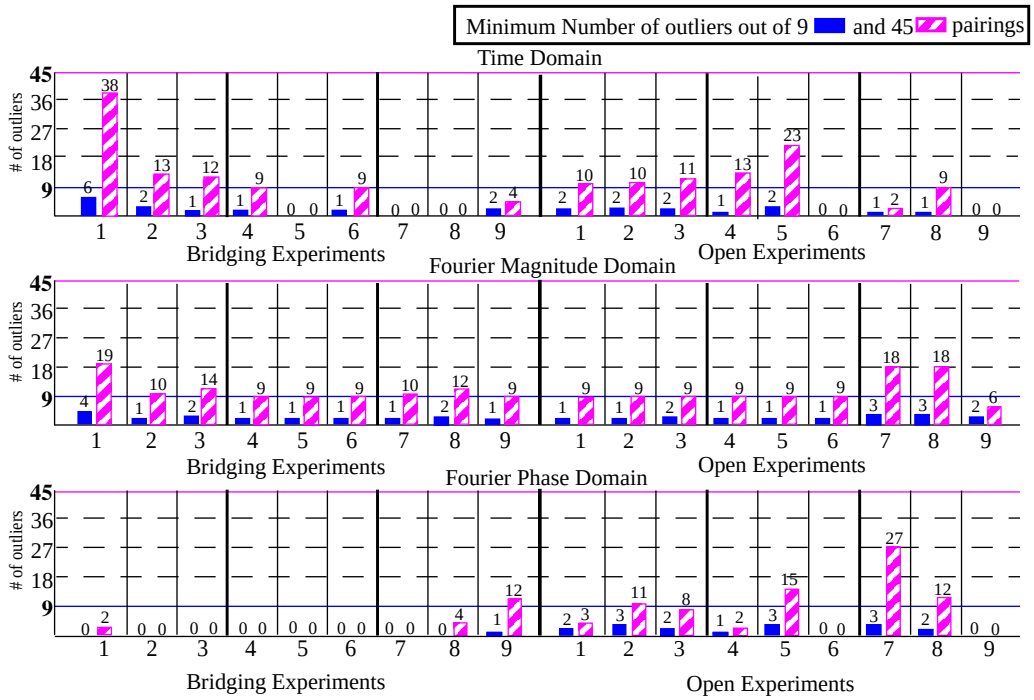

Figure 6. Time, Fourier Magnitude and Phase Nominal-Reference Results.

Vdd_1-Vdd_3, ... and pairings involving Vdd_{10}, e.g. Vdd_1-Vdd_{10}, Vdd_2-Vdd_{10}, ... If the test effectiveness metric is based on the number of experiments producing zero outliers, then the best result is obtained from the adjacent pairing analysis, which yields 5, 0 and 10 for the Nominal-Reference analysis and 5, 2 and 1 for Self-Reference analysis, as shown in the figures. The results for pairings involving Vdd_{10}, e.g. Vdd_1-Vdd_{10}, Vdd_2-Vdd_{10}, ... are 7, 0 and 13 for the Nominal-Reference and 8, 1 and 0 for the Self-Reference. However, if the test effectiveness metric is based on the **number of outliers**, the analysis of pairings involving Vdd_{10} is much larger than the number obtained for the adjacent pairing analysis. For example, the number of outliers was the maximum possible (9) for the Magnitude Nominal-Reference analysis for 16 of the 18 experiments (not shown). A similar result was obtained for the Phase Self-Reference analysis.

The transient signal behavior on Vdd_{10} is unique when compared to the other supply rails. This is illustrated by the scatter plot shown in Figure 4. The slope of the regression line is shallow (<<1) while the regression line slopes of scatter plots without Vdd_{10} are close to the expected value of 1. Since the areas computed for Vdd_{10} are plotted on the y-axis, this suggests that this supply rail topology (a circular ring, see Figure 5) is *insensitive* to process variation. In contrast, the presence of a defect causes a significant change in the transient behavior of this supply, as is evident by the elevated position of the faulted simulation data points in the figure. We are currently deriving analytical models to help explain this behavior, and hope to derive a simple test structure that will increase the sensitivity of this method to defects.

5.4 Regression Line Slope Analysis

The method as presented requires the derivation of regression lines and prediction limits for each pairing under each test sequence *a priori* using a set of known defect-free test devices. It may be possible to simplify this procedure if the regression lines and prediction limits from one test sequence can be used for other test sequences. Initial investigation of the slope of the regression lines for each of the 45 pairing across the 18 experiments show that they are well correlated and close to a value 1 for test point pairing that are topologically close (adjacent) in the layout. Of course, this excludes pairings with Vdd_{10} as discussed in the previous section. The results of the outlier analysis for pairings involving adjacent V_{dd}s presented in the histograms show that these pairings are also sensitive to defects. Therefore, this suggests that it may be possible to simplify the preprocessing procedure by starting from the assumption that the slope of regression lines from adjacent pairings is 1 under any test sequence, and proceed to derive only the prediction limits under each test sequence.

6.0 Conclusions

Transient Signal Analysis (TSA) is a parametric testing method capable of identifying defects while compensating for process variation. Using regression analysis, defect free data (perturbed by simulated process variation) is used to determine a correlation profile of a “good” device. In previ-

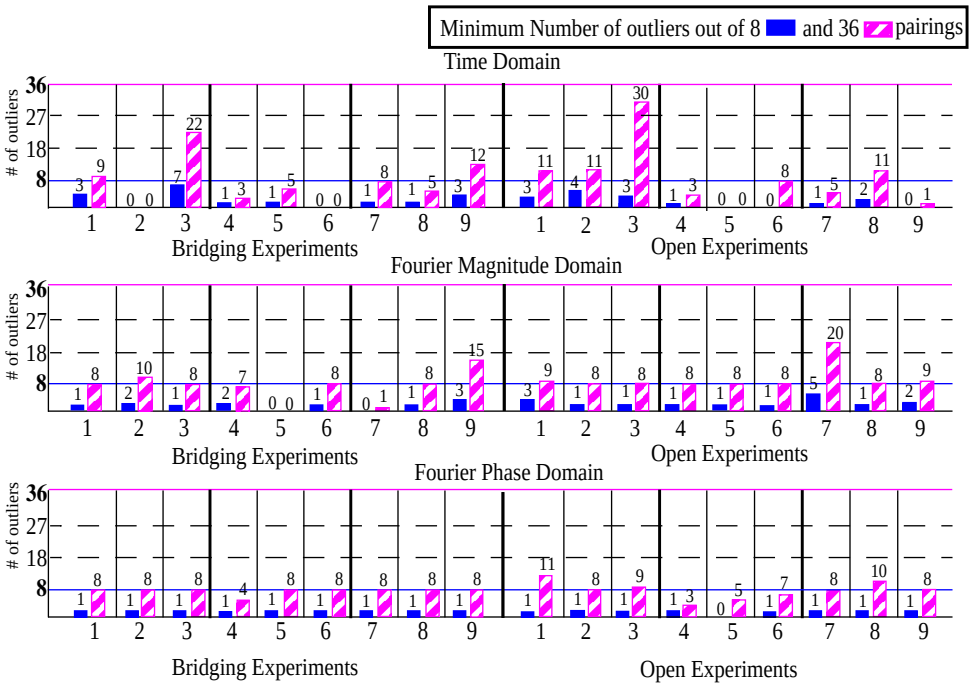

Figure 7. Time, Fourier Magnitude and Phase Self-Reference Results.

ous work, simulation experiments were conducted on defect-free simulation models of an 8-bit multiplier with injected process variation. It was shown that the detection of 18 defects was possible in 18 additional simulations conducted on a **single** 'faulted' model [3][4]. In this work, the same result is obtained over a **set** of faulted models with injected process variation. Therefore, the simulation results presented in this paper show that defect detection is possible in spite of the signal variations caused by fabrication process variations injected into either the defect-free or defective device models.

Furthermore, it is shown that the injected defects were detectable using any of several subsets of test point signals. This result and the enhanced defect sensitivity provided by the circular supply rail topology, both suggest a means of reducing the signal post-processing complexity of the method. Moreover, similarities among regression line slopes may also simplify the implementation by eliminating the need to derive a "good" device correlation profile *a priori*. The superior results shown for the self-reference analysis also suggest that the golden device profile can be relaxed or eliminated, enhancing the practicality of an implementation.

In the near future, improvements to the method will involve experiments on real circuit products and formulation of a practical implementation/approximation of the TSA technique.

Acknowledgments

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