Power Supply Transient Signal Analysis Under Real Process and Test Hardware Models

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Abstract

A device testing method called Transient Signal Analysis (TSA) is subjected to elements of a real process and testing environment in this paper. Simulations experiments are designed to determine the effects of process skew (obtained from measured parameters of a real process) on the accuracy of TSA in estimating path delays from power supply I_{DDT} and V_{DDT} waveforms. The circuit model is designed to test TSA under deep submicron process models that incorporate advanced parameters such as transistor V_t width dependencies. Modeling elements of a testing environment including the probe card are subsequently introduced as a means of evaluating the effects of tester measurement noise in an actual implementation.

1.0 Introduction

A testing method that uses power supply transient signals as a means of determining path delay characteristics of digital devices is attractive for several reasons. First, such a method may be useful in detecting resistive shorting and open defects; defects that traditionally have not been targeted by Stuck fault based methods. Second, reliable delay fault tests are difficult to generate (because of circuit hazards) and apply (because of structural tester timing accuracy). The global observability provided by power supply transient signals permits the measurement of delay without the need to sensitize paths to observation points such as Primary Outputs or scan-latches. Third, the supply transients potentially provide a higher degree of resolution than logic-based techniques with respect to the parametric characteristics of the device. This information may be useful as a means of reducing delay fault test coverage constraints. Preliminary investigations have demonstrated that a method called Transient Signal Analysis (TSA) is capable of detecting delay faults [1][2] and estimating path delays in defect-free devices [3].

The focus of this work is to determine the robustness of Transient Signal Analysis (TSA) to advanced process and tester environment elements. To this end, simulations are conducted on a circuit model derived using the measured circuit parameters of a real process. For example, the simulation RC-transistor models are based on sets of specifications sampled from the TSMC's 0.25µm process [4]. The BSIM transistor models used in this work incorporate important deep submicron parameters such as transistor V_t width dependencies. The tester environment is also simulated using advanced probe card and tester power supply models obtained from the literature [5][6]. For example, the probing environment is modeled using an advanced membrane-style probe card model. We conduct the analysis on a small circuit (dual inverter chain) that incorporates several important parameters of combinational logic paths, including fanout and transistor W/L ratios.

This paper is organized as follows. Section 2.0 describes related work. Section 3.0 presents details of the experimental circuit and the process models. Section 4.0 presents the results of simulation experiments with and without the tester environment model. Section 5.0 presents our conclusions.

2.0 Background

Vinakota et al. recently proposed a method based on the time domain analysis of power supply transients as a means of detecting delay faults in digital ICs [7]. Our technique described in [1][2] differ from previous work in several significant ways. First, the method explicitly accounts for process and vector-to-vector variation effects by cross-correlating the power supply transient signals measured at multiple supply pads simultaneously. This attribute addresses the scalability of the technique to larger devices. Second, instead of average I_{DDT}, TSA focuses on the analysis of Fourier phase harmonics. This choice is motivated by previous work which suggests that this representation is best at tracking process variation effects [2]. Lastly, the method proposed here "tracks" process variation effects but does not eliminate them. This attribute allows device parametric attributes, such as delay, to be correlated across test sequences, further reducing of possibility of test escapes.

3.0 Experimental Design

The layout of the circuit used in this paper is shown in Figure 1. The supply grid in this design is routed assuming a five layer metal process (the figure shows only the lower metal 1 and metal 2 layers for clarity). Two 2.5V power supplies tie into the power grid at the points labeled V_{DD1} and V_{DD2} in the figure. In this small layout, the wider upper layers reduced the resistance between V_{DD1} and V_{DD2} to less than 1 Ohm, making the transients at these supply points virtually indistinguishable. Therefore, the analysis that follows focuses on the waveforms obtained from V_{DD1} only.

The circuit model includes two paths implemented using chains of inverters. The heads of the two paths are labeled "Fast Path Input" and "Slow Path Input" in Figure 1. The fast path is composed of transistors with W/L ratios ranging from 2 to 5 for n-MOS and 4 to 10 for p-MOS while the slow path is composed of minimum sized transistors with W/L ratios of 1.5. The inverters along both paths fanout to as many as three other inverters in addition to the next inverter in the path. These fanout regions are labeled on the right in the figure. The diversity of transistor sizes

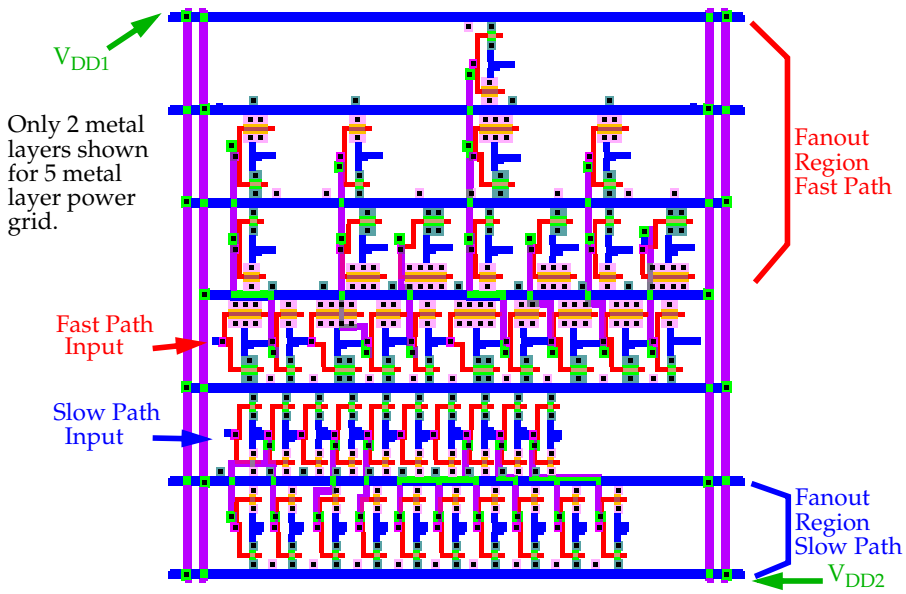

Figure 1. Layout incorporating dual paths of 10 inverters with a fast path (upper) and slow path (lower).

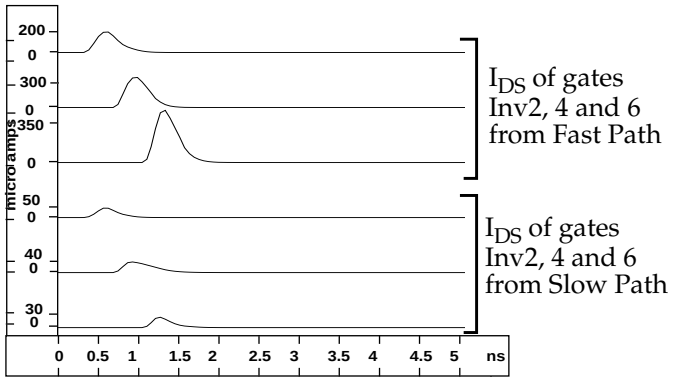

Figure 2. Sample of I_{DS} curves from simulation of layout in Figure 1.

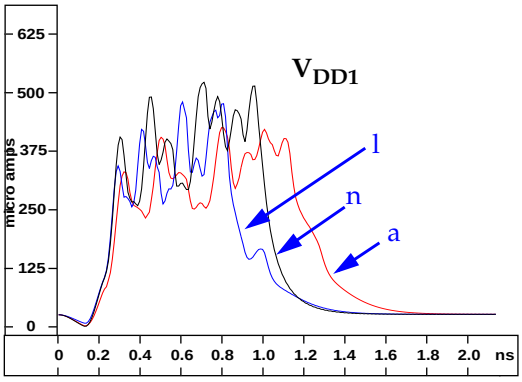

Figure 3. I_{DDT} waveforms obtained under three TSMC simulation models derived from MOSIS data.

and loading conditions causes a corresponding diversity in the I_{DS} curves of the inverters. A sample of the I_{DS} curves from one simulation model are shown in Figure 2.

The process models are derived from a set of MOSIS specifications for TSMC's 0.25µm process [4]. Each of the specifications is given as lot averaged conductor RC parasitics and BSIM modeling parameters derived from test structure measurements. At the time of this writing, 14 data sets were available. These data sets were used to configure a set of technology files for the SPACE extraction tool [8] and the corresponding SPICE simulation models were extracted from the layout. These parameter values represent worst case values because they were obtained from wafer lots fabricated over a period of several years.

The test stimulus drives both paths simultaneously, as a means of representing the more common multi-path signal propagation model of real circuits. Since the supply grid is unified, the I_{DS} curves generated by the inverters along both paths superimpose in a composite I_{DDT} curve. The composite I_{DDT} signals from three simulation models, labeled as *a*, *l* and *n*, are shown in Figure 3.

4.0 Experimental Results

4.1 Path Delay Analysis

In order to determine the relationship between path delays and the corresponding I_{DDT}s under the different process models, it is first necessary to evaluate the signal propagation characteristics along each of the two paths across the process models. As indicated previously, the same input stimulus is used to drive the inputs of the gates at the head of the two paths. Figure 4 shows the output waveforms from the last inverters of the two paths superimposed in each row. One pairing is shown for each of the 14 process models. Even though the transistor models are identical for all transistors in each circuit model, it is clear across many of these pairings that the delays between the Fast and Slow paths are not well correlated. (The vertical dotted line provides a reference point for comparison.) This is especially true for the pairings labeled *h*, *j* and *l*. Here, significant

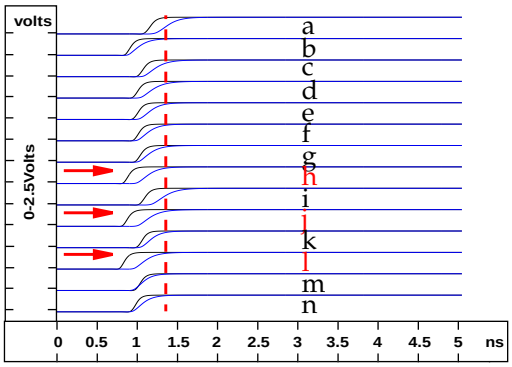

Figure 4. Path outputs: 14 TSMC process models.

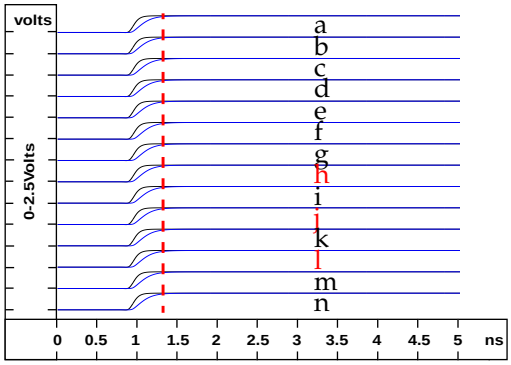

Figure 5. Path outputs: Constant bsim parameters.

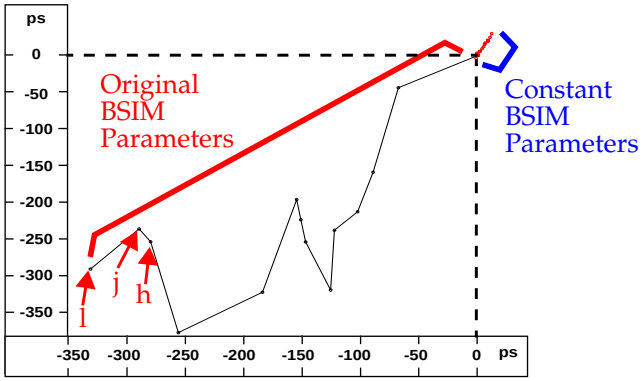

Figure 6. Slow Path relative delays vs. Fast Path relative delays taken from Figures 4 and 5.

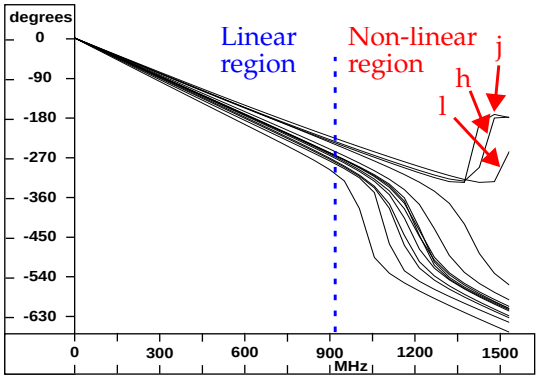

Figure 7. I_{DDT} Phase spectrums from 14 process simulations.

speed-up is observed in the Fast path delay while the Slow path delay remains relatively constant and consistent with other Slow path delays from other runs, e.g., *g*.

The lack of correlation in the delays across the output waveform pairings is largely due to the V_t dependency on transistor width (W) in the BSIM modeling equations. For example, Figure 5 shows that a much higher degree of correlation is present between these outputs when the BSIM models are held constant across the process models.

Figure 6 plots the delay characteristics of the Slow Path (y axis) against the Fast path. The delays are relative, i.e. they are computed by subtracting the absolute Slow and Fast path delays under each of the models from the corresponding absolute path delays of first (and slowest) process model, *a* (given at (0,0) in the figure). It is clear in Figure 6 that correlations between the two paths across the process models is poor. For example, the data points spanning the region labeled "Original BSIM Parameters" are poorly approximated by a straight line. In contrast, the data points spanning the region labeled "Constant BSIM Parameters" are the relative delays obtained from Figure 5. These data points span a much smaller region and are nearly co-linear.

4.2 Power Supply I_{DDT} Analysis

Even for this simple combinational circuit, the time domain representations of the I_{DDT}s are complicated by the superposition of the uncorrelated I_{DDT}s generated by the two paths as shown in Figure 3. Previous work indicates that path delays can be more easily obtained from the frequency domain representation. Of particular interest is the Fourier Phase spectrums of the I_{DDT}s since Fourier theory indicates that Phase is very sensitive to "events" in the time domain signals, such as those given by the non-linear charging currents of transistors as signals propagate. However, the lack of correlation in the delay characteristics between the two paths makes it extremely difficult to derive a single (linear) mapping function capable of tracking both path delays using either domain.

For example, Figure 7 shows the DC to 1.5GHz Phase spectrums of the I_{DDT} waveforms obtained under the 14 simulation models. A linear region and a non-linear region are separated by a vertical dashed line at 900 MHz. The non-linearity is particularly evident for the previously identified "outlier" process models *h, j, l* (see Figure 4). The relative Phase differences (shifts) are captured in the difference waveforms shown shaded to a zero baseline in Figure 8. Here, the Phase difference waveforms (also called Signature Waveforms or SWs) are computed point-wise by subtracting from the Phase spectrum of process model *a*, the Phase spectrums obtained under the other simulations. The area under the Phase SW curve is referred to as a Phase

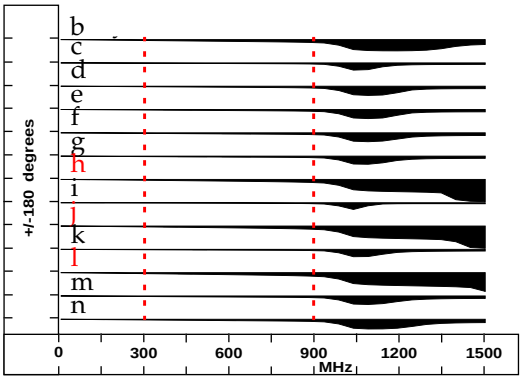

Figure 8. Phase SWs from 14 process simulations.

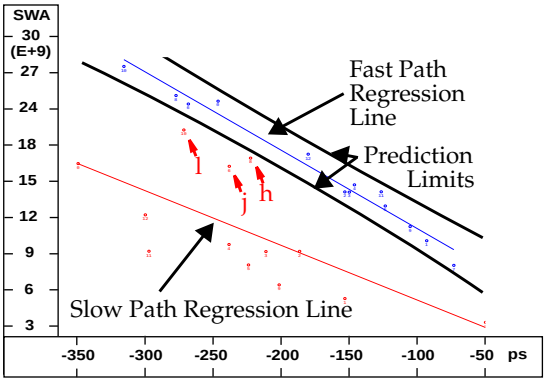

Figure 9. Phase SWAs vs. Fast (top) and Slow (bottom) relative path delays.

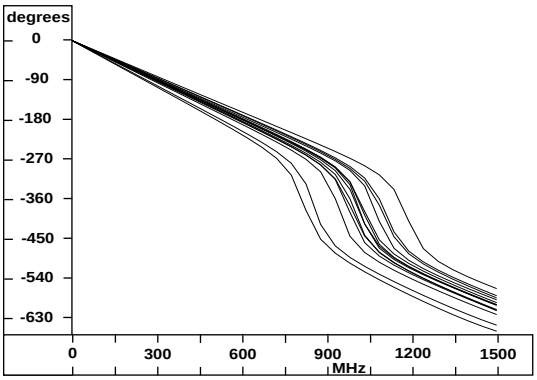

Figure 10. Unwrapped Phase spectrums from simulations under Slow Path test only.

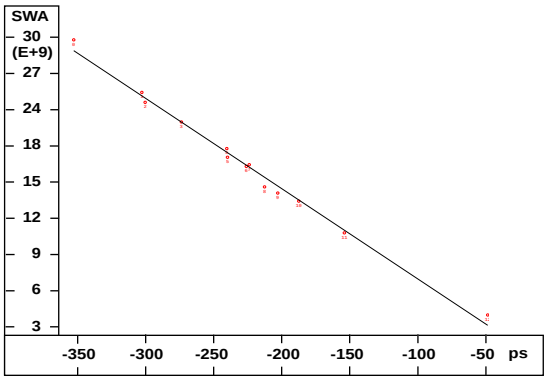

Figure 11. Phase SWA vs. relative path delays from simulations under Slow Path test only.

SWA (for Area). Since the region below 900 MHz is linear, it is reasonable to assume that this region is most likely to yield a linear mapping function between delays and Phase SWAs, if one exists. For reasons covered in the next section, these Phase SWAs are computed over an even smaller region given by 300-900 MHz.

Figure 9 shows a plot of Phase SWAs versus the relative path delays of the Fast Path (top) and Slow Path (bottom). Here, the relative path delays are computed as before, i.e. relative to the path delays obtained under simulation model *a*. The correlation of the Phase SWAs and the Fast path relative delays is stronger than the correlation of the Phase SWAs and the Slow path relative delays (prediction limits surround data points corresponding to the Fast path). The correlation coefficients for the Fast Path and Slow Path are 98.8% and 68.2% (100% is perfect correlation, e.g. the data points are co-linear). The data points labeled *h*, *j* and *l* in the figure are the least correlated in the latter mapping.

Figures 10 and 11 illustrate that the lack of correlation between the Fast and Slow path is responsible for the dispersion of the data points in Figure 9. The test used to generate the data for these figures sensitized only the Slow path. Unlike the Phase spectrums in Figure 7, the high frequency components under these simulations track more closely. Similarly, there is a much smaller dispersion of the data points in the Phase SWA vs. relative delay plot of Figure 11 when compared to the Slow path data points of Figure 9. The correlation coefficient under the single path simulations is 99.6%, versus 68.2% obtained in the dual path experiments. Similar results were obtained for the set of "Fast path only" simulations.

4.3 Power Supply V_{DDT} Analysis

The most significant problem associated with measuring the power supply current transients is related to the space constraints imposed by the physical structure of the test head. Figure 12 shows a physical model of the test head, probe card and Chip-Under-Test (CUT). Current probes, that monitor changes in the magnetic field along leads from the probe card's supply plane (see Figure 12) to the supply ports of the CUT, are likely to be too large for physical insertion. Moreover, even if such a measurement technique was possible, the built-in RC attributes of the probing apparatus and tester EMI noise sources make it difficult to accurately measure the I_{DDT} generated by the CUT. However, it may be possible to overcome these problems by measuring I_{DDT} as V_{DDT}.

Figure 12 shows the physical structure of a tester's power supplies, a Cobra (membrane) probe card and the CUT [5]. Cobra probe cards are used for wafer-level testing of CUT I/O interfaces configured in C4 pad arrays. The

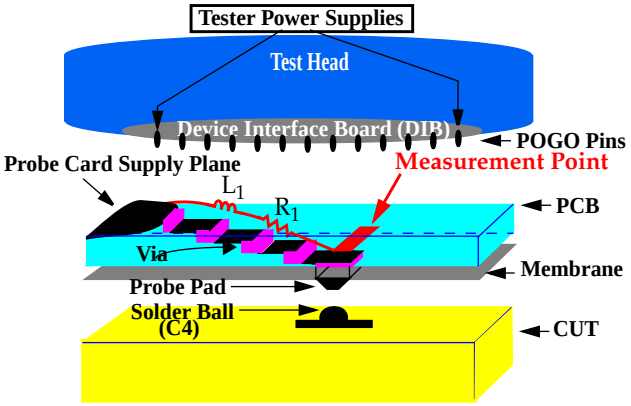

Figure 12. Tester and cobra probe card physical and electrical model.

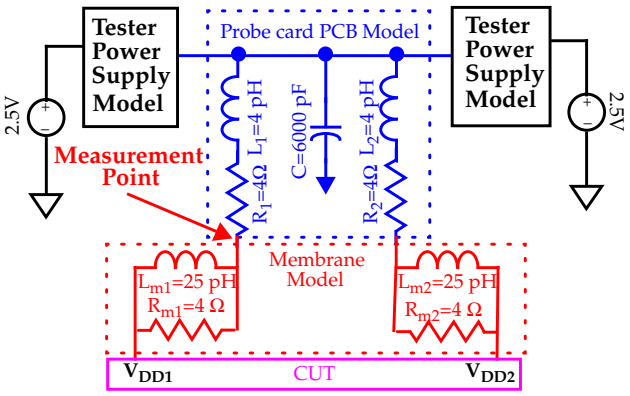

Figure 13. Testing environment RLC model.

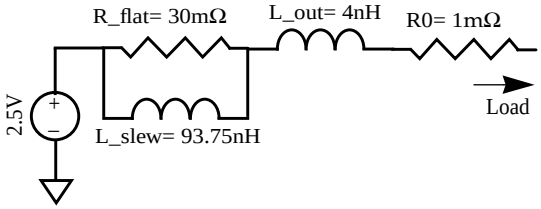

Figure 14. Voltage Regulator Power Supply Model.

tester power supplies are connected to the power plane on the probe card's PCB. This power plane is designed with a built-in capacitance of approximately 6nF, to meet the high instantaneous current requirements of the CUT. Therefore, it is difficult to measure the CUT's transient signals at any point between the power supplies and the power plane of the PCB.

Figure 12 shows a Measurement Point that may improve the accuracy of the transient signal measurements. In the figure, a wire is routed from the back edge in the lowest layer of the PCB to an internal contact connecting the membrane Probe Pad to the PCB. The PCB connection is routed up through the other layers of the PCB to the power plane in the upper-most layer. The parasitic inductance and resistance (labeled L_1 and R_1 in the figure) in the routing layers and contacts of the PCB convert the transient current to a transient voltage. These RL components "isolate" the CUT's transients from the attenuation characteristics of the Supply Plane. This type of Measurement Point insertion can be repeated for several of the power C4 pads, as a means of measuring the transients simultaneously over different regions of the CUT.

It is also possible to increase the isolation of the CUT's transients by increasing the resistance (R_1 in the figure) with a physically inserted resistor. However, only a small value of R is tolerable. This is true because the power grid on the CUT is unified and any physically inserted R is going to "divert" currents to un-monitored supply ports (which do not have the inserted R). The appropriate R needs to be chosen based on the CUT's transient current requirements and the number of monitored C4s. As shown below, a 4 Ohm resistance converts the I_{DDT} of our test circuit to a measurable V_{DDT}.

The tester/probe card RLC model used in the simulations of the inverter layout is shown in Figure 13. The values used for the PCB elements L_1 and R_1 of Figure 12 are 4 pH and 4 Ω. The Membrane Model represents the contact parasitics between the CUT's C4s and the probe card [5].

The voltage transients were measured from the Measurement Point shown in Figure 13. The Voltage Regulator RL model described in [6] and shown in Figure 14 was used to model the tester's power supply. The value of *L_slew* was changed from its original value of 67.5nH to accommodate the 2.5V supply voltage used in our simulations.

The circuit and simulation experiments performed here are described in Section 4.1. The objective here is to determine the impact of the wafer probing model. Figure 15 shows the time domain waveforms obtained from supply port V_{DD1} under three of the simulation models described previously. The low frequency sinusoidal waveform superimposed on the V_{DDT}s is generated by the model elements of the PCB and tester power supplies. The left portion of Figure 15 is blown-up in Figure 16. The similarity of these waveforms with those shown in Figure 3 suggest that the modeling elements have only a small impact on shape of the V_{DDT} waveforms.

The phase spectrums of the V_{DDT} transients obtained under the 14 simulation models are shown in Figures 17. The large sinusiodal component introduces an anomaly in the lower frequency band. The higher frequency components are very similar to those generated without the probe card model (compare with Figure 7). Figure 18 shows the phase spectrums of Figure 17 scaled along the frequency axis so as to maximize their overlap with each other. The frequency range labeled Linear Region identifies the region of interest in our analysis. The regions labeled "Divergence" identify frequency bands in which one or more of the spectra depart from the trend defined by the majority. The region labeled "Misalignment" identify the frequency

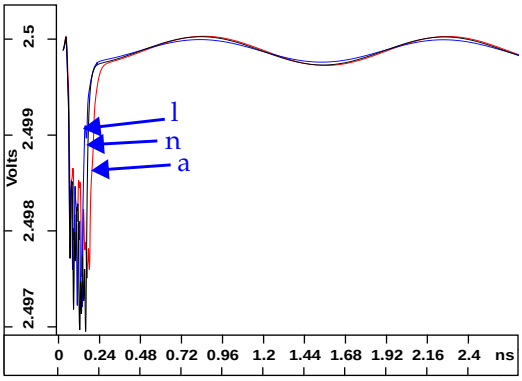

Figure 15. V_{DDT} waveforms from worst-case models.

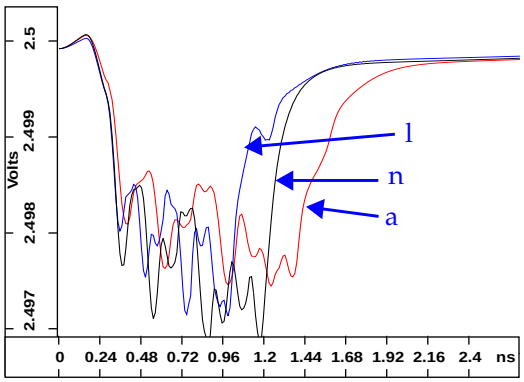

Figure 16. Magnified plot of the V_{DDT} wfms in Fig. 15.

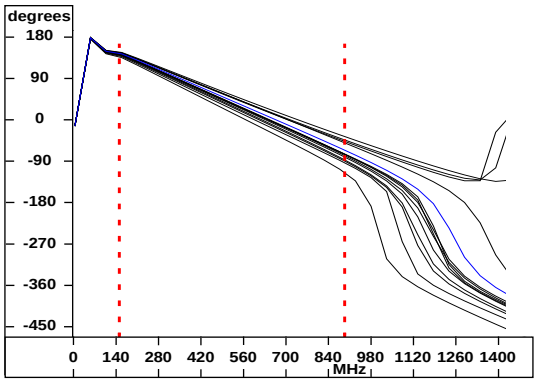

Figure 17. Phase spectrums of 14 process models.

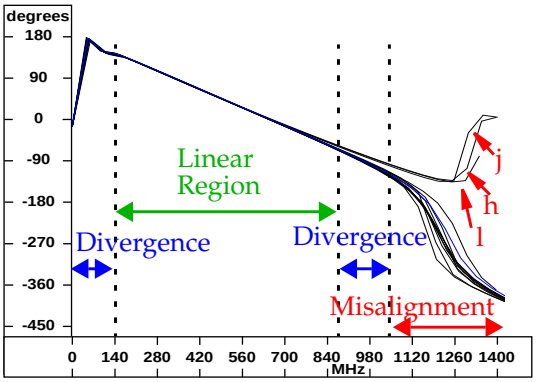

Figure 18. Frequency scaled Phase spectrums from Fig. 17.

band in which significant divergence occurs in all spectrums.

Figure 18 illustrates an important benefit of using the frequency domain representation over the time domain. The frequency domain allows regions that are not well "behaved" to be excluded from the analysis. For example, as indicated previously, the primary influence of the probe card is on the lower frequency components. The slight misalignment of the frequency components in the left-most "Divergence" region indicates that these components are likely to reduce the accuracy of the tracking between delay and Phase. The same is true in the high frequency bands above the "Linear Region".

5.0 Conclusions

This paper investigates the impact of real process and test hardware models on a testing method called Transient Signal Analysis (TSA). Low correlation of path delays can occur for paths constructed using different W/L transistor ratios in deep submicron technologies. Accurately tracking delays in these paths using test sequences that sensitize them simultaneously can be difficult using either a time or frequency domain representation of I_{DDT}. Test hardware configuration constraints indicate that the CUTs I_{DDT}s may be more easily and accurately measured as V_{DDT}s. Test hardware simulation results suggest that the electrical response characteristics of the probing structure itself tend to introduce low frequency "noise" in the supply transients. These noise factors are difficult to remove in the time domain representation of the supply transients but can be easily identified and excluded in the frequency domain analysis.

Acknowledgements

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