Hardware Results Demonstrating Defect Detection Using Power Supply Signal Measurements

Dhruva Acharyya and Jim Plusquellic

Department of CSEE, University of Maryland, Baltimore County

adhruva1, plusquel@cs.umbc.edu

Abstract

The power supply transient signal (I_{DDT}) method that we propose for defect detection analyze regional signal variations introduced by defects at a set of power supply pads on the chip under test (CUT). The method is based on the comparison of the CUT with a few chips that have been shown to be defect free. Simulation data obtained from an extracted R-model of the CUTs power grid is used to calibrate for probe card contact parasitic. Multiple defect free chips are analyzed to establish a statistical metric that distinguishes between defective behavior and process variation. This paper presents hardware results that demonstrate the effectiveness of a geometry based defect detection technique using nine copies of a test chip, eight of which were used as defect free chips and the ninth one treated as a chip with emulated defects. The method is evaluated under a variety of test scenarios to determine the sensitivity of the technique.

Introduction

Advancements in fabrication technology are posing a big challenge to conventional testing techniques [1]. Newer fabrication technologies are giving rise to new defect mechanisms. One such example is the damascene copper process in which particle related blocked-etch type of opens are quite common. Moreover clock cycles are getting shorter as the quest for higher performance chips move forward. These factors in addition to reduced timing slack, crosstalk and PWR/GND bounce increase the probability of random defects causing delay faults.

Testing techniques based on analysis of power supply signals are well suited to account for the above mentioned challenges. I_{DDQ} testing techniques have been very popular in the industry over the past decade. However, due to increase in leakage currents in DSM processes and the rise of process variation, traditional I_{DDQ} testing methods have been pushed to their limits. Moreover, I_{DDQ} testing lacks the ability to detect resistive opens which are likely to cause delay fails. I_{DDT} techniques have an advantage over I_{DDQ} techniques in this respect. However, methods based on the analysis of transient signals has its own set of challenges. Transients generated by defect free paths can overshadow the faulty transient thus rendering the defect invisible. A drawback of any I_{DDX} technique unlike any logic based technique is the "analog baggage" that naturally accompanies such methods. For example, most I_{DDT} (and I_{DDQ}) methods require a well defined threshold between good and bad chips that does not erroneously degrade yield or quality. Factors that contribute to the difficulty of defining this threshold include process variations and variations in the testing environment itself.

To overcome some of these issues, we propose a defect detection technique that uses multiple supply pad I_{DDT} signal measurements. This type of testing strategy has several advantages. The use of multiple individual supply pad measurements preserves fault detection sensitivity as chips size and transistor density increase. Second, aberrations in the individual power supply signals introduced by defects can be used to estimate the position of the defect in the physical layout of the chip [4], [15]. A significant drawback of the multiple supply pad methodology is that it is very sensitive to variations in probe card contact parasitic because this parasitic causes redistribution of currents through the different supply pads thus adversely affecting the sensitivity of our defect detection method.

In previous work, we developed and verified in hardware, a calibration method to eliminate probe card variations (and performance variations)[15]. The hardware chips analyzed in this work uses the calibration technique to eliminate anomalies due to testing environment and uses the calibrated hardware data to develop a novel defect detection technique based on analytical geometry. Our multiple supply pad defect detection technique has been able to successfully detected nearly 80% of all emulated defects spanning the entire layout of the CUT in the presence of heavy defect free activity.

Background

A variety of fault detection methods have been proposed that are based on the analysis of power supply signals [5]-[11]. The main drawback of the techniques proposed in [5]-[8] is that they do not account for vector-to-vector or process variations. Therefore, they are difficult to apply to devices fabricated in advanced technologies. The ECR I_{DDT} method accounts for process variation effects by computing ratios from the time domain I_{DDT} waveform areas measured under different test sequences [9]. The analysis presented in [14] suggests that methods based on a single test point measurement made between the probe card and the tester's power supply will not

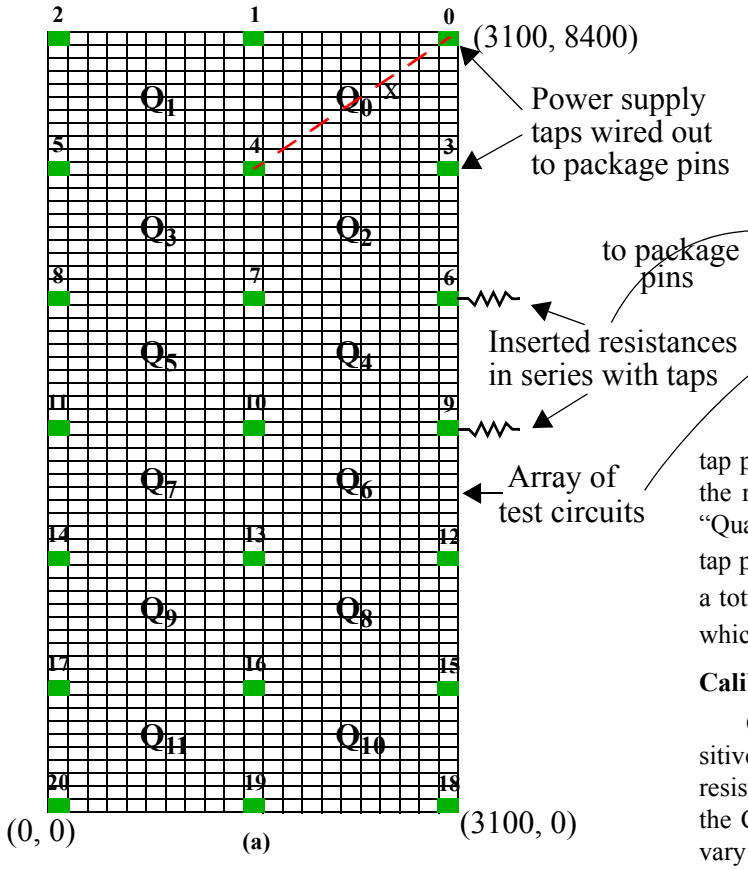

Figure 1. Test CUT.

provide adequate resolution to enable the detection of resistive defects.

Methods designed to use power supply transient signals for defect detection need to incorporate a mechanism to deal with the signal contribution introduced by defect-free signal propagation. Many test sequences will cause signals to propagate along multiple paths, increasing the difficulty of obtaining reliable detection for cases in which many of the sensitized paths are not affected by the defect. This increases the challenge of devising a general purpose method that is effective under any type of circuit topology and therefore, there are few works on this topic in the literature.

CUT Characteristics

CUT Design

A block diagram of the CUT investigated in this work is shown in Figure 1. It consists of a 60 by 21 two-dimensional array of test circuits. Each test circuit can be individually activated to provide a test stimulus to the power grid, by itself or in combinations with other test circuits in the array. The power grid is wired in two metal layers as shown in Figure 2. A set of 21 power supply taps, labeled 0 to 20 in Figure 1, emulate the multiple connection points of a typical power grid used in commercial designs. These taps will subsequently be referred to as V_{DDx} where *x* represents one of the tap connections. In order to emulate probe card contact resistance (R_p), on-chip resistances ranging from 1 Ω to 100 Ω were inserted in series between the

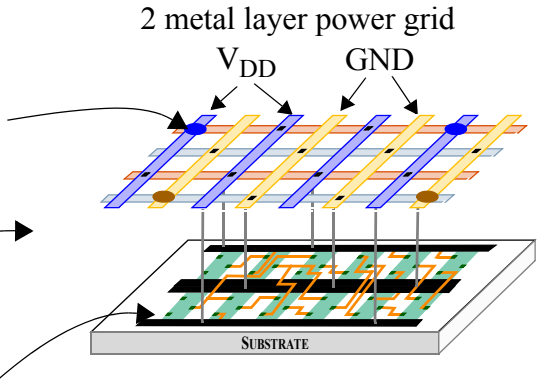

Figure 2. Test CUT's power grid. .

tap points and each of the power supply C4 pads as shown on the right side of Figure 1. The entire chip is partitioned into "Quads" which are identified as regions surrounded by 4 V_{DDx} tap points, labeled Q_0 through Q_{11} in Figure 1. Each Quad has a total of 121 test circuits (with the exception of Q_{10} and Q_{11} which have one less row.)

Calibration Circuits

Our multiple supply pad testing methodology is very sensitive to probe card contact resistance variations. The contact resistance manifests itself at the interface of the probe card and the CUT C4 solder ball. This contact resistance will not only vary from touch down to touch down but also from one supply pad to another. The contact resistance variations will manifest as anomalies in the measured distribution of the multiple supply pad currents. The presence of defects will also cause regional signal anomalies. Therefore, it is difficult to distinguish between testing environment variation and defects using only the currents measured under the logic tests.

To overcome this drawback, we introduced a DFT structure called a 'Calibration Circuit' which is described in detail in reference [16]. The basic function of the calibration circuit is to provide stimulus at known locations in the chip. Each CUT calibration cell is activated individually and the corresponding branch current measurements are made at all the supply pads. To compensate for performance variations in the calibration circuit themselves, each of the branch currents are normalized by dividing them by the total current drawn by the CUT. This data is then used in conjunction with the calibration circuit data generated from simulations to calibrate the CUT's branch currents obtained under the logic tests. The details of the procedure will be discussed in the following section. The test circuits at positions shown by the shaded blocks (the V_{DD} tap points) in Figure 1 are designated as the calibration circuits in this work. The benefit of using the calibration circuit is not limited to just calibration of probe card contact parasitic. It also forms an integral component in the analytical approach of the defect detection procedure discussed in a later section.

Calibration Procedure

As mentioned earlier, the contact resistances of the probe card will vary not only from touch-down to touch-down but also from pad to pad. The probe card contact resistance varia-

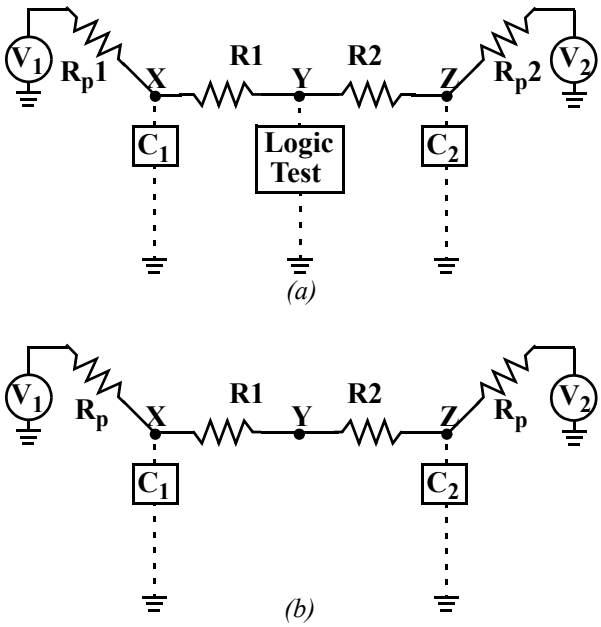

Figure 3. (a) Test Case (b) Simulation Case.

tion will distort the natural current distribution determined by the power grid alone. In order to reduce (ideally eliminate) the impact of probe resistance on the current distribution profile, it is necessary to calibrate the measured currents. In this section, we briefly illustrate the basic principles of the calibration procedure using a simple two-port network shown in Figure 3.

The circuit in Figure 3(a) represents the test case and the circuit in Figure 3(b) represents the simulation case. The test case has probe resistances R_{p1} and R_{p2} while the simulation case has a uniform probe resistance of R_p. First the calibration circuit (C_1) at location X is turned on in the test case. The currents through V_1 (I_{1CXT}) and V_2 (I_{2CXT}) are measured[1]. Similarly, currents I_{1CZT} through V_1 and I_{2CZT} through V_2 are measured by turning on calibration circuit C_2. The same procedure is performed on the simulation model generating currents I_{1CXS}, I_{2CXS}, I_{1CZS} and I_{2CZS}. I_{1T} and I_{2T} represent the currents through V_1 and V_2 respectively when a defect at location Y is provoked under a logic test in the test case. Using the eight calibration circuit measurements, the currents I_{1T} and I_{2T} can be transformed into currents I_{1S} and I_{2S} that would have been measured if the test case had uniform probe resistances of R_p.

$$\begin{bmatrix} I_{1CXT} & I_{2CXT} \\ I_{1CZT} & I_{2CZT} \end{bmatrix} \cdot \begin{bmatrix} a_1 & b_1 \\ a_2 & b_2 \end{bmatrix} = \begin{bmatrix} I_{1CXS} & I_{2CXS} \\ I_{1CZS} & I_{2CZS} \end{bmatrix} \qquad \textit{(Eq. 1)}$$

A X B

In Equation 1, matrix A contains calibration data from the test case, matrix B contains calibration data from the simulation case and the matrix X contain a set of constants that redistribute the currents measured through the multiple supply pads. This system of equations is solved to obtain the transformation matrix X by computing the inverse of A and multiplying by matrix B. Once the transformation matrix is computed, the test measurements made under a logic test are calibrated using X as shown in Equation 2. Though the expressions shown here are for a 2-V_{DD} port model, the technique can be applied to any n-V_{DD} port model.

$$\begin{bmatrix} I_{1T} & I_{2T} \end{bmatrix} \cdot \begin{bmatrix} a_1 & b_1 \\ a_2 & b_2 \end{bmatrix} = \begin{bmatrix} I_{1S} \\ I_{2S} \end{bmatrix} \qquad \textit{(Eq. 2)}$$

In the absence of grid variations and grid modelling inaccuracies, the transformation is exact. In our experiment, we created an extracted R-only netlist of the CUT's power grid and ran SPICE simulations by inserting current sources at the locations indicated as the calibration circuit locations. A uniform probe resistance value (R_p) of 1Ω was chosen for the simulations. Detailed analysis for this choice is presented in [15]. Once the test measurement data is calibrated for probe card contact resistance variations, it becomes possible to implement a reliable defect detection technique discussed in the next section.

Hyperbola Method of Defect Detection

In this work, we propose a novel defect detection procedure that is based on a geometrical model. The basic strategy underlying the fault detection method is to make use of the spatial variations in the transient signals measured individually at each power supply pads as a means of detecting the presence of a fault. Our previous work [14, 15] suggests that the power supply signal variation introduced by the defect will manifest in the surrounding supply pads proportional to the "equivalent impedance" between the defect site and each of the pads. In order to detect a fault, it is necessary to develop a reliable method of comparison between defect free chips and defective chips that accounts for process variation as well.

In previous work, we determined that the magnitude of the steady-state current (I_{DDQ}) drawn by a defect is proportional to the "equivalent resistance" between the defect site and each of the supply pads [4]. The method maps the measured I_{DDQ}s to a physical location in the layout. This technique could be extended to I_{DDT} as well. In this case, the area under the I_{DDT} waveform is used for defect detection. However, in this work we analyze average values of the measured I_{DDT} signals for the detection procedure.

The mapping procedure translates the measured multiple supply pad currents to an (x,y) layout position that represents the "center of activity" or "centroid". Under a test sequence that provokes a defect, the supply pad currents are composed of two parts, a portion due to the contribution of the defect and a portion introduced by defect-free signal propagation. The map-

1.*A note about the subscripts in I_{pqrs}: p= 1 or 2: voltage source identifier, q='C' denotes that it is a calibration test, r=X,Y,Z: location identifier and s= T,S: test case or simulation case identifier.

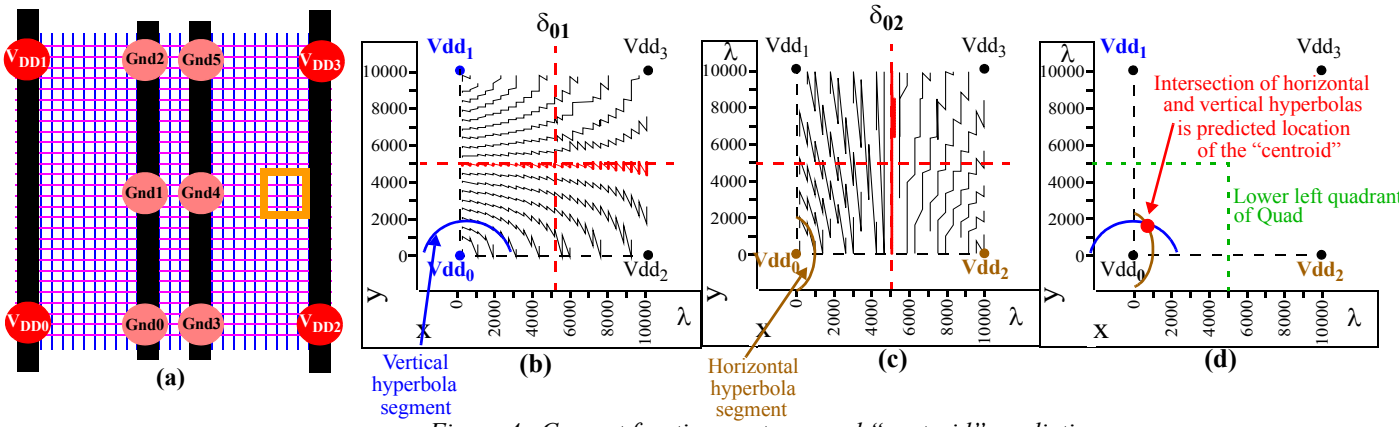

Figure 4. Current fraction contours and "centroid" prediction.

ping procedure for fault detection uses both portions in the analysis and therefore, the (x,y) coordinates returned by the mapping procedure are an abstraction that do not carry any special significance. This is true because the defect-free signal portion of the total current is likely to be generated from signal propagations that are widely distributed in the layout.

The magnitude of the I_{DDT} signal introduced by defect-free signal propagation and defects varies widely depending on the test sequence and the nature of the defect, respectively. Ideally, the layout position predicted by the mapping procedures should be independent of the signal magnitudes. To eliminate any dependence on signal magnitude, in this work, we propose **current fractions**. Here, the current fraction, δ_{xy}, defined for a supply pad pair *x* and *y* is given by Equation 3.

$$\delta_{xy} = \frac{I_x}{I_x + I_y} \qquad (Eq.\ 3)$$

In Equation 3, I_x and I_y represents the I_{DDT} signals measured through the supply pads V_{DDx} and V_{DDy} respectively. In this experiment, average I_{DDT} values are used for I_x and I_y.

In an earlier work [4], exhaustive set of spice simulations were run by inserting current sources individually at each location on a portion of a commercial power grid as shown in Figure 4(a). The portion of the power grid comprised of four VDD pads and six GND pads. The branch currents measured at each of the four VDD supply pads were used to generate the current fractions as defined in Equation 3. The current fractions for each VDD pair were sorted and contours were plotted as shown in Figure 4(b) and 4(c). Figure 4(b) shows the current fractions generated by V_{DD0}-V_{DD1} pairing whereas Figure 4(c) illustrates the contours for V_{DD0}-V_{DD2} pairing. A curve within a contour plot is all the (x,y) layout positions that produce a similar current fraction (within a small tolerance ε) for a given pair of V_{DD}s. The regularity of the contours suggested the existence of an analytical description of these curves. A model based on hyperbola were found to be adequate in describing these contours. For determining the "centroid", appropriate vertical and horizontal hyperbola curves are chosen based on the measurements made at the different supply pads and using special structures called "calibration circuits". The calibration circuits provide the maximum and minimum bounds on the current fractions that are then used to completely define the correct set of vertical and horizontal hyperbolae. The intersection of the vertical and horizontal hyperbolae indicate the location of the "centroid" in the layout as shown in Figure 4(d). Detailed mathematical analysis of the hyperbola fits can be found in [16].

The main idea behind the proposed multiple supply pad detection procedure is that it compares the "centroids" of the CUT with the "centroids" for a defect-free chip for all quads in the chip. If the defect is of significant strength, the "centroid" in at least one quad of the defective chip will be at a different location than the "centroid" for that quad in the defect free chip. To distinguish defective behavior from process variation, multiple defect free chips are analyzed. For all the defect free chips, the "centroids" in every quad will follow a distribution. We assume that the "centroid" predictions in each quad for all the defect free chips obey an elliptical gaussian distribution with independent standard deviations in the x-direction and y-direction. Under this assumption, we create an elliptical region around the cluster of defect free "centroid" predictions in every quad. The dimensions of the ellipse are determined by the 3σ values in the x ($3\sigma_x$) and y ($3\sigma_y$) directions respectively. This 3σ elliptical region around the defect free "centroid" predictions represent a "process variation zone". The 3σ ellipse becomes a circle if the standard deviations in the two dimensions become equal. If the "centroid" in any quad of the defective chip lie outside the 3σ ellipse for that quad then the defect is claimed to be detected in that quad. The defect must be detected in at least one quad of the chip in order to claim a successful detection. However, the level of confidence of detection increases if the defect is detected in more than one quad of the chip.

Hardware Experiments

Hardware experiments were conducted on nine copies of a test chip to validate the defect detection procedure described in the previous section. The average of the total I_{DDT} current and the average branch I_{DDT} currents were measured using Keithley 2400 sourcemeters as each of the test circuits on each chip was individually activated. Henceforth we will refer to

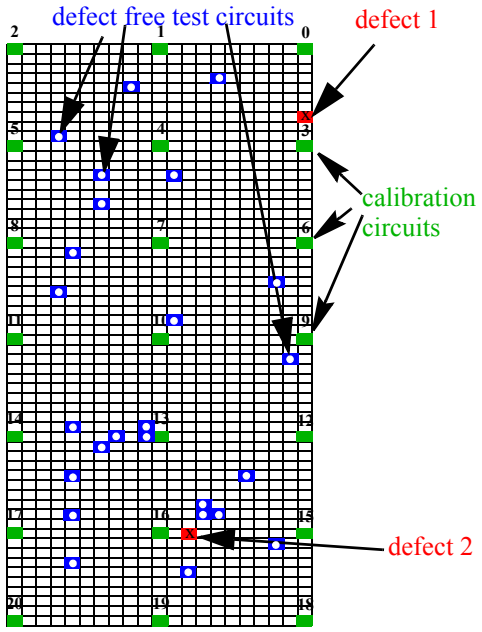

Figure 5. Distribution of 25 defect free test circuits.

these average I_{DDT} branch currents as just branch currents. The branch currents were measured using a custom board that allowed automated switching across the 21 V_{DD} ports. The total leakage and branch leakage currents were also measured in each chip. In this case, no test circuits were enabled. The leakage currents were subtracted from the currents measured with the test circuits enabled. The hardware measurements were calibrated using simulation data and hardware calibration circuit measurements.

In order to explore the sensitivity of the procedure, we constructed 11 different experiments, each experiment with a different number of test circuits activated to emulate defect free activity. The defect free cases ranged from 1 activated test circuit to 50 activated test circuits. In all the 11 test cases, the locations of the defect free test circuits were chosen randomly. To obtain, maximum flexibility in the experimental design, the test cases were not constructed by activating multiple test circuits simultaneously. Rather, the different experiments were constructed by superposing the branch current contributions of each individual test circuit. For e.g. if we desired to have "n" test circuits activated, then the total current drawn by any supply pad V_{DDx} is given by the sum of all the individual branch currents I_{VDDx} for all the "n" test circuit locations as shown in the Equation 4. The superposed branch currents were normalized by dividing by the superposition of the total currents of all the "n" test circuits to eliminate dependency on absolute signal magnitudes.

$$I_{vddx_{total}} = \Sigma I_{vddx_n} \qquad (Eq.\ 4)$$

The above mentioned experimental plan gives maximum flexibility in studying a wide range of test scenarios. A very important concern in using this strategy is that when many test circuits are activated simultaneously, there may be substantial voltage drops in the power grid which would not be accounted for when using the above scheme. Keeping this in mind, we

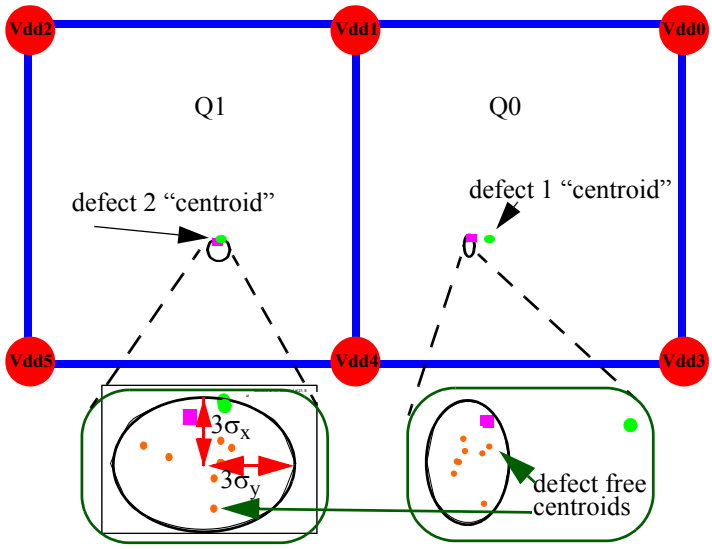

Figure 6. Centroid based detection in Q0 and Q1

conducted hardware experiments to study the amount of voltage drop in the grid as a function of the number of simultaneously activated test circuits. Our experiments indicated that about 50 test circuits can be simultaneously activated without significant potential drops in the power grid. The upper limit on the number of activated test circuits was decided by this experiment.

Figure 6 illustrates the detection algorithm for one of the experiments in which 25 randomly chosen test circuits were activated to emulate defect free activity. The locations of the activated test circuits are indicated by the "boxes with white dots" in Figure 5. A total of nine copies of the test chip were analyzed, eight of which were used as defect-free chips. The ellipses shown in Figure 6 represent the "process variation zones" for this experiment in the indicated quads. The defect free "centroid" predictions are also indicated in Figure 6. Due to space limitations, only two quads (Q0 and Q1) are shown. The ninth chip was treated as the defective chip. In this chip, each test circuit was activated individually to emulate a defect in addition to the ones that were activated for the defect free case. Henceforth we will refer to the test circuits that were used to emulate defects as defects. Figure 6 shows the "centroids" in quads Q0 and Q1 when 'defect 1' and 'defect 2' (indicated in Figure 5) were activated individually. It is clear from Figure 6 that 'defect 1' was detected in quad Q0 but not in quad Q1. 'Defect 2' was not detected in any of the two quads shown. Detailed analysis revealed that 'defect 1' was detected in four different quads (Q0, Q4, Q10 and Q11). However the maximum residual for 'defect 1' was in quad Q0. 'Defect 2' was not detected in any of the twelve quads of the test chip.

Figure 7 shows a histogram that summarizes the detection results for all eleven experiments. The x-axis in Figure 7 indicates the number of test circuits that were activated for the defect free case and the y-axis represents the number of detections. Though the CUT had 1260 test circuits, 21 of them were used as calibration circuits and the remaining 1239 were used as defects. From Figure 7, we observe that in most of the experiments, our detection technique was able to detect more than

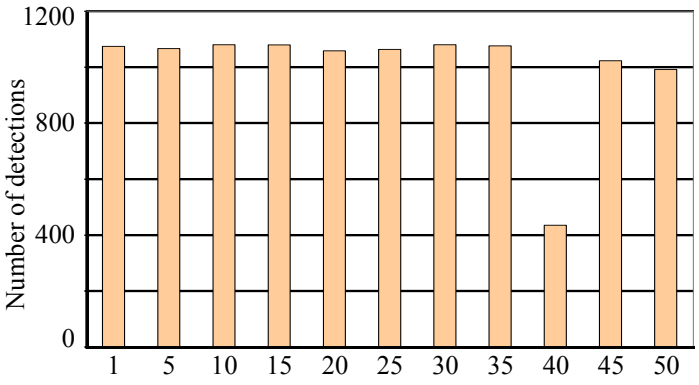

Figure 7. Detection results.

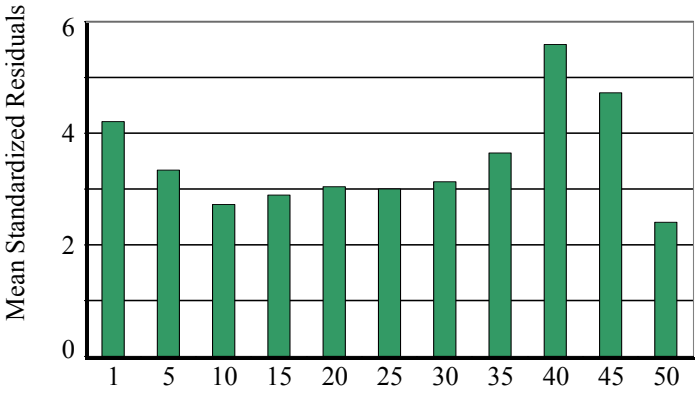

Figure 8. Mean standardized residuals

80% of the defects except for x=40 where only 35% of the defects were detected. A closer look reveals that increasing number of defect free test circuits result in less number of detections. For e.g. the number of detections from x = 1 to 35 are all above 1058, whereas for 40 it is 435, for 45 it is 1023 and for 50 it is 991. This is an expected trend because increasing defect free activity in a chip will overwhelm the effect of the defect thus making it less visible as an anomaly. In other words, the defect would not be able to pull the "centroid" significantly away from the defect free "centroids" as the amount of defect free activity increases in the chip. The number of detections for the case when 40 defect free test circuits were activated is quite lower than the other ones. This is most probably due to the distribution of defect free test circuit locations in the layout. We are currently investigating the dependency of detection sensitivity on the distribution of the defect free test circuit locations and will present the results if this work is accepted. Figure 8 shows the mean standardized residual for each of the 11 experiments indicated on the x-axis. The mean standardized residual gives a notion of the average level of confidence for all the valid detections for each experiment. Contrary to our expectations, no general trend is visible in the mean standardized residuals. The confidence associated with a positive defect detection, expressed in the magnitude of the mean standardized residual, is expected to be smaller for test scenarios in which large numbers of defect free test circuits are activated than the confidence associated with test scenarios with a smaller number of activated defect free test circuits.

Conclusions

In this paper we explored the possibilities of defect detection using average transient power supply signals. We conducted hardware experiments to validate our method. Hardware experiments show that the power grid creates regional behavior that can be used for defect detection purposes. A novel I_{DDT} defect detection technique based on geometry was implemented. Our experiments indicate that even in the presence of heavy defect free activity, the proposed method could detect, in most scenarios, almost 80% of the defects which were scattered throughout the entire layout.

Acknowledgements

We thank Anne Gattiker, Sani Nassif, Chandler McDowell and Frank Liu at IBM Austin Research Laboratory for their support in this project.

References

[1] ITRS (http://public.itrs.net/)

[2]A. Germida, Z. Yan, J. F. Plusquellic and F. Muradali, "Defect Detection using Power Supply Transient Signal Analysis", In proceedings *1999 International Test Conference*, 67-76

[3]J. F. Plusquellic, D. M. Chiarulli, and S. P. Levitan. "Identification of Defective CMOS Devices using Correlation and Regression Analysis of Frequency Domain Transient Signal Data," In proceedings *1997 International Test Conference*, 40-49.

[4]C. Patel, E. Staroswiecki, S. Pawar, D. Acharyya, and J. Plusquellic, "Diagnosis using Quiescent Signal Analysis on a Commercial Power Grid", In proceedings *2002 International Symposium for Testing and Failure Analysis*, pp. 713-722

[5]J. F. Frenzel and P. N. Marinos, "Power Supply Current Signature (PSCS) Analysis: A New Approach to System Testing", In proceedings *1987 International Test Conference*, pp. 125–135

[6]S. Su and R. Makki, "Testing Random Access Memory by Monitoring Dynamic Power Supply Current", *Journal of Electronic Testing, Theory and Applications*, Vol. 3, No 4, pp. 265-278, 1992.

[7]J. S. Beasley, H. Ramamurthy, J. Ramirez-Angulo, and M. DeYong, "I_{DD} Pulse Response Testing of Analog and Digital CMOS Circuits", In proceedings *1993 International Test Conference*, pp. 626–634.

[8]M. Sachdev, P. Janssen, and V. Zieren, "Defect Detection with Transient Current Testing and its Potential for Deep-Submicron CMOS ICs", In proceedings *1998 International Test Conference*, pp. 204-213.

[9]B. Vinnakota, W. Jiang and D. Sun, "Process-Tolerant Test with Energy Consumption Ratio", In proceedings *1998 International Test Conference*, pp. 1027-1036

[10]K. Muhammad and K. Roy, "Fault Detection and Location using I_{DD} Waveform Analysis", *IEEE Design and Test of Computers*, Volume 18, Number 1, pp. 42-49, 2001

[11]I. de Paul, M. Rosales, B. Alorda, J. Segura, C. Hawkins and J. Soden, "Defect Oriented Fault Diagnosis for Semiconductor Memories Using Charge Analysis, Theory and Experiments", In proceedings *2001 VLSI Test Symposium*, pp. 286-291.

[12]A. Singh, C. Patel, S. Liao, J. Plusquellic and A. Gattiker, "Detecting Delay Faults using Power Supply Transient Signal Analysis", In proceedings *2001 International Test Conference*, pp. 395-404.

[13]A. Singh, J. Plusquellic and A. Gattiker, "Power Supply Transient Signal Analysis Under Real Process and Test Hardware Models", In proceedings *2002 VLSI Test Symposium*, pp. 357-362.

[14] D. Acharyya and J. Plusquellic, "Impedance Profile of a Commercial Power Grid and Test System," ITC 2003, pp. 709-718.

[15]D. Acharyya and J Plusquellic, "Hardware Results Demonstrating Defect Localization Using Power Supply Signal Measurements", Accepted for publication in ISTFA 2004

[16]J Plusquellic, D. Acharyya, D. Phatak and A. Singh, "IDDT-based Fault Detection and Localization", (http://www.csee.umbc.edu/~plusquel/pubs/todaes_tsa_detect_locate.pdf).