LAB Assignment #1 for ECE 443

Assigned: Wed., Aug 27, 2008
Due: Wed., Sept 3, 2008

Description: Install and become familiar with the Xilinx ISE software distributed in class. Implement a simple combinational circuit (derived in class).

This assignment is intentionally kept very simple to allow you to get familiar with the Xilinx FPGA software tools.

Laboratory Report Requirements:

1) Turn in a commented copy of your VHDL code.
2) Turn in the schematic diagram that represents the synthesized structural representation of the code.
3) Run a simulation that shows the inputs and output behavior of the circuit.
4) Include a set of ‘sample’ waveforms in your report.

Grading:
Simple Pass/Fail grade will be assigned. Comments on your lab report will be provided.
This lab will count only as a partial lab (will be weighted much lower than subsequent labs).