LAB Assignment #2 for ECE 443

Assigned: Wed., Sept 3rd, 2008
Due: Wed., Sept 10 (Part I) and Sept 26/27 (Part II)

Description: Write the FSM for Tea Kettle. Simulate to verify in Part I. Implement on the V2Pro for Part II.

A description of Tea Kettle's behavior is as follows:

- States: Idle, Check, Heat, Delay
- Input Signals: StopStart, MinLevel, MaxLevel, Boiling, TimeOut
- Output Signals: EmptyAlarm, TooFullAlarm, Element, Timer

FSM transitions:

- Stay in Idle while StopStart == 0
- Transition to Check when StopStart == 1, return to Idle if StopStart == 0
- If MinLevel == 1,set EmptyAlarm to 1. If MaxLevel == 1, then set TooFullAlarm to 1. Remain in Check. If MinLevel == 0 && MaxLevel == 0, set EmptyAlarm to 0, set TooFullAlarm to 0 and transition to Heat. Set Element to 1.
- In Heat, if StartStop == 0, return to Idle. Stay in Heat while Boiling == 0. If Boiling == 1, set Timer to 1, transition to Delay.
- In Delay, set Element to 0. Remain in Delay while TimeOut == 0. When TimeOut == 1, set Timer to 0 and transition to Idle.

Part I: Laboratory Report Requirements:

1) Turn in a commented copy of your VHDL code.
2) Turn in the schematic diagram that represents the synthesized structural representation of the code.
3) Run a simulation that shows the inputs and output behavior of the state machine.
4) Include labeled waveforms for all transitions in your report.

Grading:
60% VHDL code correctly specifies desired functionality.
10% Meaningful comments in VHDL code.
30% Meaningful simulation results.

Part II: Laboratory Requirements

FMAC demonstration on the FPGA boards. The inputs of the FSM must be mapped to the buttons on the Spartan 3 and V2Pro's and the outputs to the leds. You are free to choose the specific mapping. During the demo, you need to demonstrate that your FSM makes the appropriate transitions. We will ask you to show the state of the registers defining the FSM using ChipScope.

Grading:
100%: Degree of correct operation of the FSM.