LAB Assignment #3 for ECE 443

Assigned: Wed., Sept 17th, 2008
Due: Wed., Sept 24 (Part I) and Oct 1 (Part II)

Description: Implement a UART port on the FPGA.

Part I: Type in the UART code discussed in class and given in the text including the loop-back circuit given on page 176.

Part I: Laboratory Report Requirements:

1) Turn in a commented copy of your VHDL code.
2) Turn in the schematic diagram that represents the synthesized structural representation of the code.
3) Run a simulation that demonstrates proper operation of the UART port.
4) Include labeled waveforms for all transitions in your report.
Grading:
60% VHDL code correctly specifies desired functionality.
10% Meaningful comments in VHDL code.
30% Meaningful simulation results.

Part II: Laboratory Requirements

Demonstrate the UART port working with Windows Hyperterminal or putty.exe. Further details will be discussed on Sept 24th.

Grading:
100%: Degree of correct operation of the FSM.