LAB Assignment #4 for ECE 443

Assigned: Wed., Oct 8th, 2008
Due: Wed, Part I: Oct 22, Part II: 24/25

Description: Transfer a file using the UART to and from the FPGA.

Use one of the discussed methods to add an SRAM block of 10K bytes to the working UART code that you completed last week. Write a state machine that takes the data received from the UART on the FPGA and stores it in the SRAM. The transfer to the FPGA will be accomplished with hyperterminal -- use hyperterminal to select an ASCII file to send. The end of the transfer will be designated by the standard end of file ASCII character used for Windows files (ASCII character hex *1a*. Once received, the state machine will switch into transmit mode. **You can switch to transmit mode once the EOF character is received OR you can wait for a button press on the FPGA board.** Once the button press is received, the state machine should begin sending the file (in the same order) back to hyperterminal or putty.

NOTE: DO NOT USE A FIFO -- USE BRAM. For example, if you use the CoreGen program, after setting the parameters for the FPGA chip, you get a menu of CORES that are available for your chip. Select ‘Memories & Storage’, ‘RAMs & ROMs’ (NOT FIFO) and then ‘Block Memory’. The Block Memory Generator dialog then appears, choose ‘Single Port RAM’ (the default), leave ‘Minimum Area’ selected for the Algorithm, click ‘Next’. Set ‘Memory Size’ params ‘Write Width’ to 8 and ‘Write Depth’ to 1024, leave ‘Operating Mode’ set to ‘Write First’, ‘Enable’ set to ‘Always Enabled’ and ‘Output Reset Value’ at 0. Click ‘Next’. The next screen allows you to add a register to the output of the BRAM ‘DOUTA[7:0]’ under ‘Optional Output Registers’ ‘Port A’ -- this can be used to improve performance but for this assignment, it is not needed so leave the defaults -- nothing selected. Leave ‘Memory Initialization’ at its default value. The next screen enables various simulation options -- leave them at their default values. Click Finish.

Part I: Laboratory Report Requirements: (Due 10/22/08)

1) Turn in a commented copy of your VHDL code.
2) Turn in the schematic diagram that represents the synthesized structural representation of the code.
3) Run a simulation that demonstrates proper operation of the UART port.
4) Include labeled waveforms for all transitions in your report.
Grading:
60% VHDL code correctly specifies desired functionality.
10% Meaningful comments in VHDL code.
30% Meaningful simulation results.

Part II: Laboratory Requirements (Due: 10/24 or 10/25)

Demonstrate the file transfer code on your FPGA using Windows hyperterminal or putty.exe.

Grading:

100%: Degree of correct operation of the FSM.