LAB Assignment #5 for ECE 443

Assigned: Wed., Nov 5th, 2008
Due: Wed, Part I: Nov 7/8, Part II: Nov 12/14/15

Description: VGA code for pong game.

Part I: Create a project with the code that I give on my web site and try it out on the FPGA. The code describes a low level VGA driver that generates the hsync, vsync and comp_sync signals for the monitor. The parent (vga_sync_test) generates the rgb signals and simply changes the background color of the screen. Be prepared to demonstrate **at least** this code by this Friday/Saturday. As I indicated in class, I would strongly suggest that you modify this code to include some version of the pong game, either the static version where nothing moves or the dynamic version that I demonstrated in class. Any extras beyond what is given in the book, for example, adding a score keeping feature, will count as extra credit during the demonstration. There is no lab report required for Part I.

Part II: Type in the code from my slides (or the book) that implements the ping game with a moving round ball and paddle. Replace the pushbutton that control the paddle movement (bar) with the UART that you coded in Lab 3 & 4. Assign an two keys on the keyboard (your choice) to control the up-down movement of the paddle. Turn in a lab report to Craig next Wednesday (Nov 12) that lists your code, gives a high level block diagram that shows how the modules are connected together (with signal names for wires connecting the modules). If you choose to document simulation results (not required), then that will count as extra credit as long as you indicate very clearly what is occurring, i.e., don't just turn in a simulation diagram with your signal names; annotate (with a pen/pencil) what is going on. There are lots of other ways to get extra credit, e.g., by adding features that you'll need for the space invader project (which follows this lab). In fact, changing pong to render graphics for the space invader game will count as extra credit. Be prepared to demonstrate your code in hardware on Nov. 14 & 15.

Pick a partner for the project and email me your choice by next Wednesday (Nov 12).

Part I: Laboratory Report Requirements: (Due 11/12/08)

1) Turn in a commented copy of your VHDL code.
2) Turn in the block diagram as described above, hand drawn is okay.
3) Optional extra credit: Run a simulation that demonstrates the VGA + UART code. You must CLEARLY indicate what is occurring in the waveform diagram by written annotation (see above).
Grading:
80% VHDL code correctly specifies desired functionality.
20% Meaningful comments in VHDL code.
Extra: 10 pts -- meaningful simulation results.

Part I & II: Laboratory Requirements (Due: 11/7-8 and 11/14-15)

Demonstrate your VGA + UART code on your FPGA.
Grading: 100%: Degree of correct operation of your code.