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SoC Interconnection: Wishbone

Description

The WISHBONE System-on-Chip (SoC) Interconnect Architecture for Portable IP Cores is a portable interface for use with semiconductor IP cores. Its purpose is to foster design reuse by alleviating system-on-a-chip integration problems. This is accomplished by creating a common, logical interface between IP cores. This improves the portability and reliability of the system, and results in faster time-to-market for the end user. WISHBONE itself is not an IP core...it is a specification for creating IP cores.

OpenCores recommends the WISHBONE System-on-Chip Interconnect as the interface to all cores that require interfacing to other cores inside a chip (FPGA, ASIC, etc.).

The WISHBONE standard is not copyrighted, and is in the public domain. It may be freely copied and distributed by any means. Furthermore, it may be used for the design and production of integrated circuit components without royalties or other financial obligations.

News

07-09-2002, OpenCores Releases WISHBONE Rev.B3 specs.

12-08-2002, Silicore transfers WISHBONE Stewardship to OpenCores. See press release

Aditional information

Download a copy of the WISHBONE, Revision B.3 Specification - Adobe Acrobat *.PDF, 920KB.

A WISHBONE Service Center page is available at:
www.silicore.net/projects.cgi/web/projects.cgi/web/wishbone.htm

Comparison to other SoC buses

- Review of Three SoC Buses by Rudolf Usselmann soc_bus_comparison.pdf (79 Kb)
- List of other SoC buses www.silicore.net/uCbusum.htm

Application notes

- appnote_01.pdf (21 Kb)

Research opportunities

WISHBONE offers an excellent opportunity for engineering professionals and students

to contribute to SoC research. Research topics of interest to the WISHBONE community include (but are certainly not limited to):

- Interconnection practices for point-to-point interfaces.
- Interconnection practices for shared bus architectures.
- Interconnection practices for crossbar switches.
- Interconnection practices for off-chip routing.
- Interconnection IP cores of all types.
- Benchmarking methods for FPGA and ASIC devices.
- Benchmarking circuits.
- Benchmarking data.
- Effects of specific circuit design practices on system throughput.
- Automatic generation of WISHBONE interfaces (e.g. for DSP cores).

If you have an interesting paper that you've written or any other information of general interest, please send it to the WISHBONE Steward (below). If it's presented well, then we'll add it to this site so that others can learn from your work. Submissions should not be copyrighted, or include a copyright release for publication on this site.

Maintainer

Stewardship for the WISHBONE specification is maintained by Richard Herveille. Questions, comments and suggestions about the document are welcome, and should be directed to rherveille@o....

The WISHBONE document is currently not available under the OpenCores CVS system. It was felt that that this would make too many versions of the standard available, thereby degrading it into a set of more-or-less useless documents. However, the long term plan is to move stewardship for the document to a public standards body.