LAB Assignment #1 for ECE 443

Assigned: Mon., Aug 31, 2009
Due: Mon., Sept. 9, 2009

Description: Implement a simple combinational circuit that maps the push-buttons to LEDs.

This assignment is intentionally kept simple to allow you to get familiar with the Xilinx FPGA software tools. The tutorial already covered using the pushbuttons and LEDs. In this assignment, you will extend the tutorial to a (slightly) more interesting project.

You will use the four pushbuttons, UP, DOWN, LEFT and RIGHT as input and the four LEDS, LED 3, LED 2, LED 1 and LED 0 as output. NOTE: Both the Buttons and LEDs are active low -- a '1' in table for input means 'Btn pressed' and a '1' for output means LED is on. Write the structural VHDL code necessary to realize the following mapping:

INPUT (When pressed, BTNs output '0')				**OUTPUT (LED on when driven to '0')**			
UP	DOWN	LEFT	RIGHT	LED 3	LED 2	LED 1	LED 0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
0	1	0	0	0	0	1	0
0	0	1	0	0	0	1	1
0	0	0	1	0	1	0	0
1	1	0	0	0	1	0	1
1	0	1	0	0	1	1	0
1	0	0	1	0	1	1	1
0	1	1	0	1	0	0	0
0	1	0	1	1	0	0	1
0	0	1	1	1	0	1	0

Laboratory Report Requirements:

1) Turn in a commented copy of your VHDL code.
2) Turn in the schematic diagram that represents the synthesized schematic of the code.
BONUS points (10 pts):
a) Run a simulation that shows the inputs and output behavior of the circuit.
b) Include a set of 'sample' waveforms in your report.

Grading:
Your lab grade will consist of two parts. The first part is associated with the in-class demo, and is worth 50% of the total grade (50 pts). Successful demonstration of the lab's stated requirements is worth 50 pts. Partial implementations will be given only partial credit. The second portion of the lab grade is derived from your lab report. Correct implementation counts for 30 pts (of the 50 pts). The remaining 20 pts will be given according to how well the VHDL code is written and documented (comments). Bonus points will be given to any implementation feature that goes above and beyond the requirements.