LAB Assignment #2 for ECE 443

Assigned: Wed., Sept 9, 2009
Due: Mon., Sept. 16, 2009

Description: Write a test bench and simulate the following behavioral description of lab #1 that maps the push-buttons to LEDs.

This assignment is again intentionally kept simple to allow you to get familiar with the Mentor Graphics simulation tools. You will need to complete the following process statement to implement the logic description from lab #1 and then write a test bench and simulate.

```
-------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Entity declaration (I NEED MORE COMMENTS -- HELP!)
entity push_to_led_behav is
   Port ( up, down, left, right : in  STD_LOGIC;
          led_out : out  STD_LOGIC_VECTOR (3 downto 0)
   );
end push_to_led_behav;

-- Architecture
architecture Behavioral of push_to_led_behav is
signal button_bus: std_logic_vector(3 downto 0)
   begin

   button_bus <= up&down&lef&right;
   process (button_bus)
      begin
      led_out <= "1111";
      if (button_bus = "0111" or button_bus = "1101" or button_bus = "0011" or
          button_bus = "0110" or button_bus = "1010" ) then
          led_out(0) <= '0';
       end if;

       (ADD REST OF CODE HERE)

   end process;
end Behavioral;
```

Laboratory Report Requirements:

1) Turn in a commented copy of your VHDL code along with a schematic.
2) Write a test bench and run simulation(s) that shows the inputs and output behavior of the circuit (be sure to include a set of 'sample' waveforms in your report).
Grading:
Your lab grade will be derived from your lab report. Correct functional behavior is worth 50 pts. Evidence of simulation, e.g, waveforms included in your report, is worth 20 pts. The remaining 30 pts will be given according to how well the VHDL code is written and documented (comments). Bonus points will be given to any implementation feature that goes above and beyond the requirements.