LAB Assignment #2 for ECE 443

Assigned: Wed., Sept. 8, 2010
Due: Wed., Sept. 15, 2010

Description: Study UART code and run a simulation

The objective of this assignment is to expose you to a design unit, in this case, a UART. A UART is hardware component that implements serial communication between two entities, e.g., the FPGA and your laptop. You are not required to write any VHDL code for this assignment but rather just download the code under the lab2_files link, create a project and run a simulation on the provided test bench. We will discuss the UART in class so you become familiar with its operation. Although many of the constructs in the vhdl code will be unfamiliar to you, you should study and try to understand its basic operation.

Laboratory Report Requirements:

None: Demo simulation in class on the due date.