LAB Assignment #3 for ECE 443

Assigned: Mon., Oct. 19, 2015 Due: Wed., Oct. 21, 2015

Description: Copy the code from the VGA lecture on slides 37 to 53 and demonstrate a working pong game.

- 1) NOTE: You'll need to modify the top level port to work with the 12 VGA color signals. Top level entity of code in slides has 24 bit color (you have only 12).
- 2) Note that you will have 3 modules, pont_top_st, vga_sync_unit and pong_grf_st_unit.

Study this code carefully. It will define the basis for your game.

Laboratory Report Requirements:

Grading:

The grading from this lab will be based entirely on your in-class demo. Bonus points will be given to any implementation feature that goes above and beyond the requirements. Please print out and turn in a copy of your VHDL code.