LAB Assignment #0, Part 1, for ECE 338

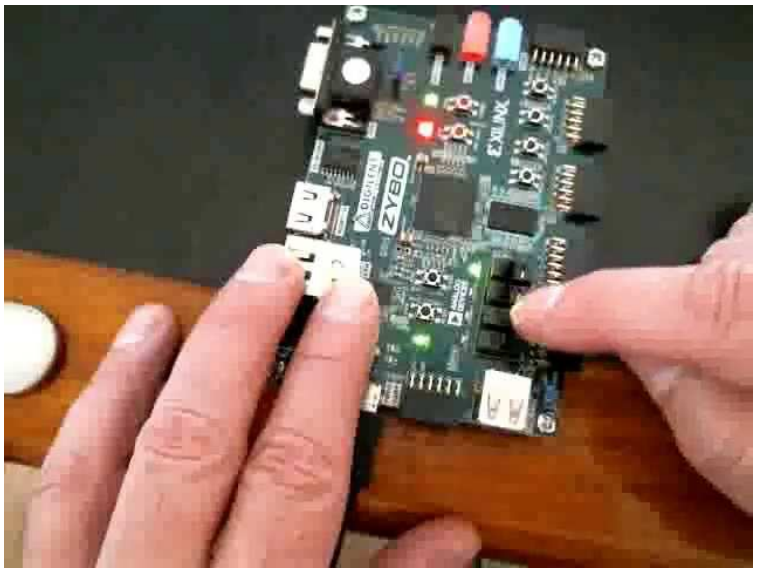
Assigned Aug 29th
Due Sept 5th

Description: Implement and demo a PL-side version of the full adder with switches and leds as input and output

Use the Vivado instruction screencasts to install Vivado, create a project, synthesize a design, generate a bitstream and program the FPGA. Implement a full adder in your VHDL code using the following entity declaration

```
entity full_adder is
    Port ( a : in STD_LOGIC;
           b : in STD_LOGIC;
           ci : in STD_LOGIC;
           co : out STD_LOGIC;
           sum : out STD_LOGIC);
end full_adder;
```

Be prepared to demo in class.



This lab is worth 10 points and only involves a hardware demo.