LAB Assignment #2, for ECE 338

Assigned Sept 17th
Due Sept 19th

Description: Create a project with behavioral VHDL and evaluate the behavioral-to-hardware translation process.

Use Vivado to create a project. Add the following VHDL code which uses an 'indexed' simple assignment within a process block. Open 'elaborated design' and identify components of the schematic that correspond to elements of the VHDL code. Please keep your lab report to 1 page, and include your name and the title "Lab #1: Behavioral-to-Schematic Translation, index statement". DO NOT EMAIL ANY LAB REPORTS. Print them out and give them to me in class.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity Index is
   Port (
      ctrl: in std_logic_vector(1 downto 0);
      a: out std_logic_vector(3 downto 0)
   );
end Index;

architecture rtl of Index is

signal au: unsigned(3 downto 0);
begin

   process (au, ctrl)
      begin
      au <= (others=>'0');

      au(to_integer(unsigned(ctrl))) <= '1';

      a <= std_logic_vector(au);

      end process;

end rtl;
```

This lab is worth 10 points and requires a quick hardware demo.