LAB Assignment #9, for ECE 338

Assigned Nov. 7th
Due Nov. 12th

Description: Download the HDMI driver project, synthesize and run it.

Combine labs 7, which includes the processor, BRAM, GPIO, with lab8, which includes an MMCM and the HDMI_driver code.

Replace the connection of 'sys_clk' with 'FCLK_CLK0'. You should double click on the Zynq processor in the block diagram, click 'Clock Configuration', expand 'PL Fabric Clocks' and ensure that FCLK_Clk0 **is set to 100 MHz**. NOTE: this is a change from what we discussed in class. It is not clear why 50 MHz does NOT work. The frequency of FCLK_CLK0 appears to remain at 100 MHz no matter what you set the frequency to, so leave it at (or explicitly set it to) 100 MHz.

Double click on the 'clk_wiz_0', under the Board tab change the 'sys_clk' to 'Custom' in the Board Interface column. Under Clocking Option tab, the Primary Input Clk field 'Input Frequency' should be set to 'Auto' and should show 100.00. Save and validate the Block diagram.

Use the 25 MHz output Clk0 from the clk_wiz_0 as the clock for nearly all of the components in the block diagram as we discussed in class.

Also, courtesy of Ivan, you can create you Top.vhd module with the HDMI, GPIO and BRAM defined in the entity as you did in lab7 and lab8, add it to the project and then drag-and-drop from the sources window to the block diagram window. You can then use the wiring tool in the block diagram to connect up the components. Doing it this way avoids the need to edit and modify the design_1_wrapper.vhd file as we have been discussing in class and in the screencasts!

You will need to generate the design_1_wrapper.vhd file after validating the block diagram.

Prepare a demo that shows the screen being updated with the switches from lab8 and the C program output from lab7.

This lab is worth 20 points and requires a quick hardware demo.