LAB Assignment #0, for ECE 338

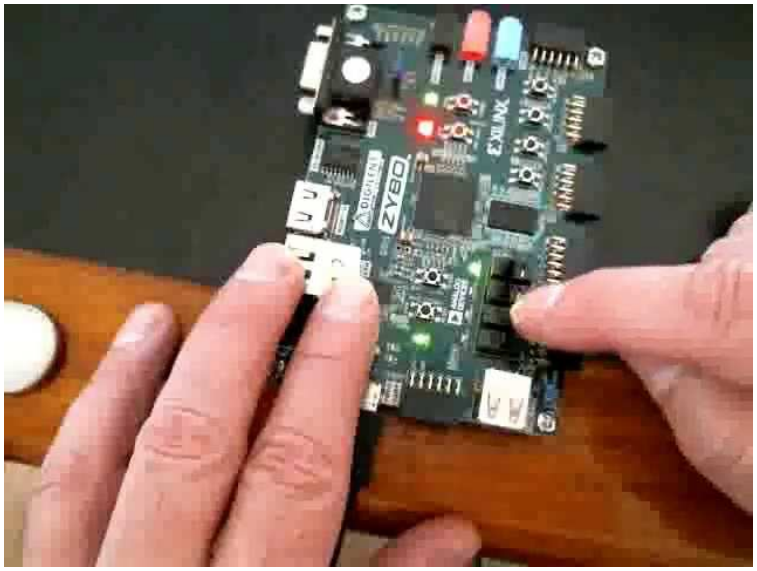
Assigned Sept. 4th
Due Sept 9th

Description: Implement and demo a PL-side version of the full adder with switches and leds as input and output

Use the Vivado instruction screencasts to install Vivado, create a project, synthesize a design, generate a bitstream and program the FPGA. Implement a even detector in your VHDL code using the following entity declaration

```
entity even_detector is
   port(
      a: in std_logic_vector(2 downto 0);
      even: out std_logic
      );
   end even_detector;
```

Be prepared to demo in class.



This lab is worth 10 points and only involves a hardware demo.