LAB Assignment #3, for ECE 338

Assigned Sept 18th
Due Sept 23th

Description: Create a project with behavioral VHDL and evaluate the behavioral-to-hardware translation process.

Use Vivado to create a project. Add the following VHDL code which uses priority MUX based constructs. Open 'elaborated design' and identify components of the schematic that correspond to elements of the VHDL code. Synthesize and open 'schematic', and identify components. Are there any significant differences? Please keep your lab report to 1 page, and include your name and the title "Lab #1: Behavioral-to-Schematic Translation, Priority MUX constructs". DO NOT EMAIL ANY LAB REPORTS. Print them out and give them to me in class.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity PriorityMUX is
   Port (
      inputs: in std_logic_vector(3 downto 0);
      ctrl: in std_logic_vector(3 downto 0);
      leds: out std_logic_vector(1 downto 0)
   );
end PriorityMUX;

architecture rtl of PriorityMUX is

begin
-- Priority MUX via conditional signal assignment
   leds(0) <= inputs(0) when ctrl(0) = '1' else
              inputs(1) when ctrl(1) = '1' else
              '0';
   process (inputs, ctrl)
      begin
         leds(1) <= '0';

-- Priority MUX via if assignment
         if ( ctrl(2) = '1' ) then
            leds(1) <= inputs(2);
         elsif ( ctrl(3) = '1' ) then
            leds(1) <= inputs(3);
         end if;
      end process;
end rtl;
```

This lab is worth 10 points and requires a software demo.