LAB Assignment #5, for ECE 338

Assigned Sept 30th
Due Oct 2nd

Description: Create a Block Diagram with the Zynq processor, 1 dual-channel GPIO and a 8 KB BRAM.

Use Vivado to create a project. Create a block diagram.

- Click '+', search Zynq, select Zynq7 processing system
  - Run 'Connection automation'
  - Click okay (NO changes)

- Click '+', search GPIO, select AXI GPIO
  - Run 'Connection automation'
  - Check 'axi_gpio_0', and click okay.
  - Double click on the GPIO

  Configure the GPIO with 2 channels, with channel 1 configured as a 32-bit input register and channel 2 configured as a 32-bit output register as follows:
  - Change the 'Board Interface 'from btns 4 bits' to 'Custom'
  - Click 'IP Configuration' tab
  - Leave 'All Inputs' checked
  - Change GPIO Width of GPIO to 32
  - Click 'Enable Dual Channel'
  - For GPIO 2, Check 'All Outputs'
  - Make sure GPIO Width is set to 32
  - Click okay to close the configuration dialog
  - Do NOT run 'Connection Automation'
  - Click on pin 'btns_4bits' and change name in 'External Interface Properties' to 'GPIO_Ins'
  - Right click on 'GPIO2' near the '+' sign (cursor turns to pencil)
  - Select 'Create Interface Port'
  - Change 'Interface name' to 'GPIO_Outs'

- Click '+', search BRAM, select 'Block Memory Generator'

  Configure a memory with 8 KB words, where each word is 16-bits wide as follows:
  - Double click on the BRAM_PORTA but NOT ON THE NAME -- ON THE BLOCK
  - In the Block Memory Generator dialog, set Mode to Stand Alone
  - Click 'Port A Options' tab
  - Set 'Write Width' to 16
  - Leave 'Write Depth' set to 8192
  - Select 'Always Enabled' under 'Enable Port Type'
  - Uncheck 'Primitives Output Register'
  - Click 'okay'
  - Right click on 'BRAM PORTA' near the '+' sign (cursor turns to pencil)
  - Select 'Create Interface Port'
  - Leave name set to BRAM_PORTA
  - Click 'okay'

- Add clock and reset as ports as follows:
  - Right click on FCLK_CLK0 on ZYNQ (cursor turns to pencil)
  - Select ‘Create Port’
  - Leave name as ‘FCLK_CLK0’
  - Right click on FCLK_RESET0_N
  - Select ‘Create Port’
  - Leave name as ‘FCLK_RESET0_N’

Click ‘Validate Design’ (square with check mark in it). Ignore the 4 critical warning.
Type <Ctrl-S> to save the block diagram.
Clock the Block Diagram (click ‘x’ in upper right hand corner.
Right click ‘design_1 in Source window.
Select ‘Create HDL Wrapper’
Click ‘Copy generated wrapper to allow user edits’
Click ‘okay’.
‘design_1_wrapper.vhd’ displays.

Turn in a screen snapshot of your block diagram and vhdl ‘wrapper’ file (only the top portion of your ‘wrapper’ vhdl file needs to be shown in your screen snapshot).

This lab is worth 10 points.