LAB Assignment #7, for ECE 338

Assigned Oct 7th
Due Oct 14nd

Description: Create an mixed C code/VHDL project that allows user data to be transferred between the PS and PL sides.

Use Vivado to create a project, add the block diagram as discussed in lab5 and lab6, add the VHDL code that I have supplied, synthesize the project and program your FPGA with the bitstream. The VHDL code implements a VHDL state machine that reads and/or writes a portion of the 8K 16-bit word BRAM. The state machine is controlled from a C program through the two GPIO registers. The low order 16 bits of these registers also serve as a mechanism to transfer 16-bit data words between the C program and the VHDL state machine.

NOTE: You should double click on the Zynq processor in the block diagram, click 'Clock Configuration', expand 'PL Fabric Clocks' and reset FCLK_Clk0 from 100 to 50 (MHz).

Create an application in SDK and import the C file I have provided on my website for this lab. The C program reads a data file (also supplied) and transfers it, one 16-bit word at a time, to the GPIO register. As it does so, the VHDL state machine reads the GPIO register and stores it in the BRAM. Once the C program has loaded the memory with data, a second routine is called that simply unloads it, one 16-bit word at a time and then prints the results.

Run the application with the datafile that I've provided. Create a screen snapshot of the printed output from your run of the program.

This lab is worth 20 points and requires a quick hardware demo.