LAB Assignment #8, for ECE 338

Assigned Oct. 21st
Due Oct. 23rd

Description: Download the HDMI driver project, synthesize and run it.

Download the tcl-based project or the Vivado project (courtesy of Charles), synthesize it and then be prepared to demo it using the monitors in 215. Charles has posted instructions on his github site if you decide to use the tcl-based project. Toggle the switches to change the color scheme on the screen.

NOTE: The build.tcl script only creates the project. You need to run synthesis, implementation and bitstream generation using the Vivado gui.

The script is currently set up to work with 2017.2. Please change the following

1) Search and change 2017 to 2018 in build.tcl

2) Search and change 2017.2 to 2018.2 in z7_hdmi_driver/src/bd/design_1.tcl

2) Comment clk_wiz:5.4 out and add clk_wid:6.0 as shown below in z7_hdmi_driver/src/bd/design_1.tcl

```
# Create instance: clk_wiz_0, and set properties
#  set clk_wiz_0 [ create_bd_cell -type ip -vlnv xilinx.com:ip:clk_wiz:5.4 clk_wiz_0 ]
#  set_property -dict [ list \
#CONFIG.CLKOUT1_JITTER {165.419} \
#CONFIG.CLKOUT1_REQUESTED_OUT_FREQ {25} \
#CONFIG.CLKOUT2_JITTER {119.348} \
#CONFIG.CLKOUT2_PHASE_ERROR {96.948} \
#CONFIG.CLKOUT2_REQUESTED_OUT_FREQ {125} \
#CONFIG.CLKOUT2_USED {true} \
#CONFIG.CLK_IN1_BOARD_INTERFACE {sys_clock} \
#CONFIG.CLK_OUT1_PORT {clk_slow} \
#CONFIG.CLK_OUT2_PORT {clk_fast} \
#CONFIG.MMCM_CLKOUT0_DIVIDE_F {40.000} \
#CONFIG.MMCM_CLKOUT1_DIVIDE {8} \
#CONFIG.MMCM_DIVCLK_DIVIDE {1} \
#CONFIG.NUM_OUT_CLKS {2} \
#CONFIG.USE_BOARD_FLOW {true} \
#CONFIG.USE_LOCKED {false} \
#CONFIG.USE_RESET {false} \
# ] $clk_wiz_0
#
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:clk_wiz:6.0 clk_wiz_0
```

```
endgroup
set_property -dict [list \
CONFIG.CLKOUT2_USED {true} \
CONFIG.CLKOUT1_REQUESTED_OUT_FREQ {25} \
CONFIG.CLKOUT2_REQUESTED_OUT_FREQ {125} \
CONFIG.MMCM_DIVCLK_DIVIDE {1} \
CONFIG.MMCM_CLKFBOUT_MULT_F {10.000} \
CONFIG.MMCM_CLKOUT0_DIVIDE_F {40.000} \
CONFIG.CLK_IN1_BOARD_INTERFACE {sys_clock} \
CONFIG.CLK_OUT1_PORT {clk_slow} \
CONFIG.CLK_OUT2_PORT {clk_fast} \
CONFIG.MMCM_CLKOUT1_DIVIDE {8} \
CONFIG.NUM_OUT_CLKS {2} \
CONFIG.CLKOUT1_JITTER {175.402} \
CONFIG.CLKOUT1_PHASE_ERROR {98.575} \
CONFIG.CLKOUT2_JITTER {125.247} \
CONFIG.CLKOUT2_PHASE_ERROR {98.575} \
CONFIG.USE_BOARD_FLOW {true} \
CONFIG.USE_LOCKED {false} \
CONFIG.USE_RESET {false}] \
[get_bd_cells clk_wiz_0]
```

This lab is worth 10 points and requires a quick hardware demo.