LAB Assignment #9, for ECE 338

Assigned Oct. 23th
Due Oct. 30th

Description: Download the HDMI driver project, synthesize and run it.

Combine labs 7, which includes the processor, BRAM, GPIO, with lab8, which includes an MMCM and the HDMI_driver code.

a) Begin by copying lab8 z7_hdmi_driver VHDL code and the Vivado project to lab9. Preserve the hierarchy just as it existed in lab8.

b) Make a directory in lab9 called VHDL and C_code, exactly as you had it in lab7. Copy the lab7 VHDL files (**Top.vhd**, **LoadUnloadMem.vhd** and **DataTypes_pkg.vhd**) to lab9 VHDL directory. Do the same for the C_code directory -- copy all the files to lab9.

c) Edit **VHDL/Top.vhd** and add the port definitions from **top.vhd** in the hdmi directory (**z7_hdmi_driver/src/top.vhd**). Be sure to copy **hdmi_red, hdmi_green, hdmi_blue, hdmi_hzync, hdmi_vsync, hdmi_enable, sw_r, sw_g, sw_b**.
You do NOT need to copy the **clk** and **reset** signals since they already exist in **VHDL/Top.vhd** as **Clk** and **reset**. Don't forget to add a '**;**' to one of the port lines after you add the new entity ports otherwise you'll get a syntax error.

d) Copy the **hdmi_sync** component (if you have one) and the instantiation from **z7_hdmi_driver/src/top.vhd** to **VHDL/Top.vhd**. Put the component above the **begin** statement in the architecture definition and the instantiation below the **begin**. Also copy the three assignment statement to **hdmi_reg, hdmi_green and hdmi_blue** just below the instantiation. Basically, you are copying everything except for **clk** and **reset** from **z7_hdmi_driver/src/top.vhd** into **VHDL/Top.vhd**.

e) Save **Top.vhd**.

f)Run vivado from the lab9 vivado directory and open the project. Do the following:
1) Remove **design_1_wrapper.vhd** from the project.
2) Replace **top.vhd** under **Top_0/design_1_top_0_0/top.vhd** with **Top.vhd** (the file you just edited above). You will NOT use **top.vhd** at all.
3) Add **DataTypes_pkg.vhd** and **LoadUnloadMem.vhd** to the project.
4) You should see the following:
U0: Top(beh) (Top.vhd)(2)
LoadUnLoadMemMod: LoadUnLoadMem(beh)(LoadUnLoadMem.vhd)
hdmi_sync_i: hdmi_sync(rtl)(hdmi_sync.vhd)

g) Open the block diagram. You should see lab8's block diagram with the hdmi component. Add the Zynq processor, GPIO and BRAM as you did for lab7 to the block diagram, and configure them exactly the same way.

h) Run automation to automatically add the **rst_ps7_0_50M** and **ps7_0_axi_periph** blocks. Be sure **FCLK_CLK0** from the Zynq IP block is connected to **M_AXI_GP0_ACLK** on the **processing_system7_0**, the three **ACLK** pins on the **ps7_0_axi_periph** block and the **slowest_sync_clk** on the **rst_ps7_0_50M** block.

i) Double click on the **processing_system7_0** to configure it, Click Clock Configuration and expand PL Fabric Clocks. Set **FCLK_CLK0 Requested Frequency** to 100 MHz (it is 50 MHz by default). You MUST do this -- there used to be a bug in Vivado which may or may not be fixed now. Close the Zynq configuration dialog.

j) Delete the **sys_clk** pin, which connects to **clk_in1** of the **clk_wiz_0**. Connect **FCLK_CLK0** on **processing_system7_0** to **clk_in1** on **clk_wiz_0**.

k) Double click **clk_wiz_0** to configure it. Set the Board Interface from **sys_clk** to **Custom** under the Board tab. Click Clocking Options tab and make sure Primary says 100 MHz (should be set automatically). Close the dialog. (NOTE: You may need to upgrade the IP from last year using the Tools/Report/Report IP Status menu to report the status and then clicking the upgrade selected IP button along the bottom).

l) Delete all existing ports except for **hdmi_out**, **DDR**, **FIXED_IO**.

m) Drag and drop **Top.vhd** from Sources to the block diagram. This should create a IP block called **Top_0**.

n) Connect the **hdmi_red/green/blue** ports on **Top_0** to the **In0/1/2** ports on **xlconcat_0**.

n) Expand the **RGB** port on **rgb2dvi_0**. Connect **hdmi_hzync** on **Top_0** to **vid_pHSync** on **rgb2dvi_0**. Do the same for **Top_0** ports **hdmi_vsync** (to **vid_pVSync**) and **hdml_enable** (to **vid_pVDE**).

o) Connect **clk_slow** from **clk_wiz_0** to **Clk** on **Top_0**, to **clka** on **blk_mem_gen_0** and to **PixelClk** on **rgb2dvi_0**.

p) Connect GPIO ports on **axi_gpio_0** to corrresponding ports on **Top_0**, as in lab7.

q) Connect **blk_mem_gen_0** ports to correponding ports on **Top_0**, as in lab7.

r) Right click on **reset** pin on **Top_0** and select 'create port'. CLICK ON THE **reset** port and select 'active high'. YOU MUST DO THIS!!! This should eliminate the bubble on the **reset** pin on **Top_0**.

s) Right click on each of the **sw_r, sw_g** and **sw_b** pins on **Top_0** and create port.

t) Validate and save the block diagram. Generate **design_1_wrapper.vhd**.

u) Right click on **design_1_wrapper** and 'select as Top'. You MUST do this!!!

Prepare a demo that shows the screen being updated with the switches from lab8 and the C program output from lab7.

This lab is worth 20 points and requires a quick hardware demo.