LAB Assignment #0, for ECE 338

Assigned Sept. 7th
Due Sept. 13th

Description: Implement and demo a PL-side version of the full adder with switches and leds as input and output

Use the Vivado instruction screencasts to install Vivado, create a project, synthesize a design, generate a bitstream and program the FPGA. Implement a even detector in your VHDL code using the following entity declaration

```
entity even_detector is
   port(
      a: in std_logic_vector(2 downto 0);
      even: out std_logic
      );
   end even_detector;
```

Note: The video references the ZYBO board, XDC file, etc. The exact same process occurs for the Cora board. However, the Cora board has ONLY two push buttons on the board (no switches) and therefore, please use btn[0] and btn[1] from the Master XDC file. Uncomment and change the names of btn[0] and btn[1] in the XDC file to a[0] and a[1] as described in the video, respectively. For a[2], connect it to Pmod Header JA pin Y18 (directly below the btn definitions in the XDC file), i.e., uncomment and rename ja[0] to a[2]. You will not be able to control the state of this input -- it is not a button or switch, and so it will remain at 0. Please just demonstrate with the two pushbuttons and ignore a[2] since it cannot be controlled from the board.

Include two pictures of your FPGA with the leds showing two different states.

This lab is worth 10 points and only involves a hardware demo.

NOTE: ALL ASSIGNMENTS MUST BE UPLOADED THROUGH UNM LEARN AS PDF FILES. Do NOT submit WORD docx files or any other format but PDF. You will be able to upload as many times as you like until the assignment is graded. You may be penalized as I describe in the syllabus for late assignments so please submit your best effort by the due date.