LAB Assignment #3, for ECE 338

Assigned Oct 10th
Due Oct 12th

Description: Create a project with behavioral VHDL and evaluate the behavioral-to-hardware translation process.

Part A: Use Vivado to create a project. Add the following VHDL code which uses priority MUX based constructs. Open 'elaborated design' and identify components of the schematic that correspond to elements of the VHDL code. Synthesize and open 'schematic', and identify components. Are there any significant differences? Please include your name and the title "Lab #3: Behavioral-to-Schematic Translation, Priority MUX constructs".

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity PriorityMUX is
   Port (
      inputs: in std_logic_vector(3 downto 0);
      ctrl: in std_logic_vector(3 downto 0);
      leds: out std_logic_vector(1 downto 0)
   );
end PriorityMUX;

architecture rtl of PriorityMUX is

begin
-- Priority MUX via conditional signal assignment
   leds(0) <= inputs(0) when ctrl(0) = '1' else
              inputs(1) when ctrl(1) = '1' else
              '0';
   process (inputs, ctrl)
      begin
         leds(1) <= '0';

-- Priority MUX via if assignment
         if ( ctrl(2) = '1' ) then
            leds(1) <= inputs(2);
         elsif ( ctrl(3) = '1' ) then
            leds(1) <= inputs(3);
         end if;
      end process;
end rtl;
```

Part B: Use Vivado to create a project. Write your own VHDL code which uses a case statement and one or more if-else-endif statements within the case statement, all within a process block describing combinational logic, to implement a function (your choice), where the entity outputs are a function of the entity inputs (remember, if you do NOT connect your VHDL statement inputs and outputs to the entity inputs and outputs, Vivado will simply delete the statements you write). You are allowed to change the entity inputs and outputs names, size and directions to anything you like, i.e., they do NOT need to use those given in the VHDL of part A above. But you are not permitted to copy VHDL from any other assignments or from other publicly available sources. Open 'elaborated design' and identify components of the schematic that correspond to elements of the VHDL code. Please title "Lab #3: Behavioral-to-Schematic Translation, Case and If-Else-Endif Statements".

This lab is worth 20 points.