LAB Assignment #5, for ECE 338

Assigned Oct. 17th
Due Oct. 24th

Description: Create a project with behavioral VHDL and evaluate the behavioral-to-hardware translation process.

Part A: Use Vivado to create a project. Add the VHDL code which implements the multiplier FSMD from the lecture. Open 'elaborated design' and identify components of the schematic that correspond to elements of the VHDL code. Please include your name and the title "Lab #5: Multiplier FSMD from Lecture".

Part B: Use Vivado to create a project. Write your own VHDL code which instantiates the multiplier FSMD from Part A and implements the following:
1) Idle: It checks the ready signal, if '1', it applies two 8 bit values of your choice to the 8 bit inputs of the multiplier and asserts the start signal and transitions to the WaitMultDone state.
2) WaitMultDone: It continuously checks the status of the ready signal. If ready becomes '1' again, it transitions back to Idle. Please title "Lab #5: Multiplier FSMD with Parent Module".

This lab is worth 20 points.