# ECE 338: Intermediate Logic Design

**Course:**

ECE 338: Intermediate Logic Design, Fall 2019. 3 credits.

**Course Instructors:**

Prof. Jim Plusquellic
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Office Hours: by appointment

**Optional Text:**

RTL Harware Design Using VHDL: Coding for Efficiency, Portability, and Scalability, Pong P. Chu, ISBN-13: 978-0-471-72092-8 ISBN-10: 0-471-72092-5

**Optional supplementary text:**

FPGA Prototyping By VHDL Examples, Xilinx Spartan-3 Version, Pong P. Chu, ISBN: 978-0-470-18531-5

**Grading:**

The distribution of weights for the exams, homeworks and projects is as follows:

| Component | PCT |
|---|---|
| Final | 25% |
| Labs | 35% |
| Project | 35% |
| Class Participation | 5% |

No incompletes will be given, except as required by university policy for truly exceptional circumstances.
Students are encouraged to participate in class.

**Cheating at any time in this course will cause you to fail the course.**

**For a complete description of academic dishonesty, refer to the UNM Student Handbook.**

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**Course Outline:**

| Date | Lecture |
|---|---|
| Week 1 | Introduction |
| Week 2 | Overview of VHDL |
| Week 3 | Overview of VHDL |
| Week 4 | Concurrent Signal Assignment Stmts |
| Week 5 | Concurrent Signal Assignment Stmts |
| Week 6 | Sequential Statements in VHDL |
| Week 7 | Sequential Statements in VHDL |
| Week 8 | fall break |
| Week 9 | Finite State Machines |
| Week 10 | Finite State Machines |
| Week 11 | Register Transfer Methodology |
| Week 12 | Register Transfer Methodology |
| Week 13 | Register Transfer Methodology |
| Week 14 | Thanksgiving |
| Week 15 | Register Transfer Methodology |
| Week 16 | Project Demos |
| | Final exam |

(Note: Changes/Additions to this schedule will be posted on my web site http://www.ece.unm.edu/~jimp)