International Technology Roadmap for Semiconductors

1999 Edition

Introduction

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FOREWORD

The semiconductor industry has continued to prosper and also to foster the growth of multiple industries since the early 70s. At the center of this sustained growth, resides the unique factor that has made the semiconductor industry successful: "Decreases in device feature size have provided improved functionality at a reduced cost." Device linear features have indeed decreased at the rate of about 70% every three years for most of the industry's history. Acceleration to a 2-year cycle has been experienced in the most recent years. Cost per function has simultaneously decreased at an average rate of about 25–30%/year/function.

Since 1992, the Semiconductor Industry Association (SIA) has coordinated the efforts of producing what was originally the *National Technology Roadmap for Semiconductors* (NTRS). This document of requirements and possible solutions was generated three times: in 1992, 1994, and 1997. The NTRS has provided a 15-year outlook on the major trends of the semiconductor industry. As such, it has been a good reference document for all semiconductor manufacturers. Most of all, it has provided useful guidance for suppliers of equipment, materials and software. It has also provided clear targets for researchers in the outer years.

The semiconductor industry has become a global industry in the '90s, as many semiconductor suppliers have established manufacturing or assembly facilities in multiple regions of the world. Similarly, the suppliers to the semiconductor industry have established world-wide operations. Furthermore, alliances, joint ventures, and many forms of cooperation have been established among semiconductor manufactures as well as among equipment, materials, and software suppliers.

The above considerations have led to the realization that a document that provides guidance for the whole industry would benefit from inputs from all regions of the world that have leadership activities in the field of semiconductors. This realization has led to the creation of the *International Technology Roadmap for Semiconductors* (ITRS). The invitation to cooperation on the ITRS was extended by the SIA at the World Semiconductor Council in April of 1998. The offer was enthusiastically accepted by the trade organizations of Europe (EECA), Korea (KSIA), Japan (EIAJ), and Taiwan (TSIA). The initial collaboration of these five organizations produced the ITRS 1998 Update, which consisted of a comprehensive revision of the 1997 NTRS tables. This year, the five regions have jointly produced a new edition of the semiconductor industry roadmap document—*The International Technology Roadmap for Semiconductors: 1999.*

As the reader will realize by studying this newly created document, the number and the difficulty of the technical challenges continue to increase as technology moves forward. The red areas signifying: "No solutions yet" are in most cases shown within a 5-year reach. Traditional scaling, which has been at the basis of the semiconductor industry for the last 30 years, is indeed beginning to show the fundamental limits of the materials constituting the building blocks of the planar CMOS process. However, new materials can be introduced in the basic CMOS structure to replace and/or augment the existing ones to further extend the device scaling approach. Since the assimilation of these new materials into the modified CMOS process gives the device physicist and the circuit designer improved electrical performance similar to the historical trends, this new regime has been often identified as "Equivalent Scaling." It is expected that these new materials will provide a viable solution to extending the limit of the planar CMOS process for the next 5–10 years.

Despite the use of these new materials, it will be challenging to maintain a rate of improvement in electrical performance of about 2× every two years in the high-performance components by relying exclusively on improvements in technology. Innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement. To achieve this result it is expected that the integration of multiple silicon technologies on the same chip and a closer integration of package and silicon technology will be necessary. This emerging product category is identified as Performance System-on-a-Chip (P-SoC).

On the other hand, cost-effective solutions will require an assessment of the silicon technology complexity that can be afforded for a given cost. Specifically, given a system cost target, what technology complexity can be afforded? This product category is identified as Cost-effective System-on-a-Chip (C-SoC).

Finally, as the ITRS looks at 10–15 years in the future, it becomes evident that most of the known technological capabilities will be approaching or have reached their limits. In order to provide the Computer, Communication, Consumer, and other electronics industries with continuously more efficient building blocks, it becomes necessary to investigate new devices that may provide a more cost-effective alternative to planar CMOS in this timeframe. Adequate preparation for this potential transition must include starting to identify the possible candidates as early as possible and, then, systematically testing their feasibility.

In conclusion, note that the planar CMOS silicon gate technology ultimately resulted from technical investigations initiated in the 1940s. These early studies did not lead to the start of the semiconductor industry, as we know it today, until the late 60s. It would be difficult for any single company to support the progressively increasing R&D investments necessary to evolve the technology from Traditional Scaling to Equivalent Scaling, and, finally, to investigate and develop a set of new devices usable beyond the limits of CMOS. The contributors to the ITRS agree that much of the R&D needs to be in the shared "pre-competitive domain."

It is the purpose of this 1999 ITRS to provide a reference document of requirements, potential solutions, and their timing for the semiconductor industry. This result has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university and government labs. It is hoped that, in the future, starting with this document as a common reference and through cooperative efforts among the various ITRS participants, the challenge of R&D investments will be cooperatively and more uniformly shared by the whole industry.

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The Semiconductor Industry Association wishes to formally and sincerely express its appreciation for the many hours of tremendous personal effort involved to deliver this collection of information. The devotion and attention given by each individual contributor of the Roadmap represents perhaps the greatest enabling energy within our industry.

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INTRODUCTION

OVERVIEW

The 1999 edition of *The International Technology Roadmap for Semiconductors (ITRS)* is the result of a worldwide consensus building process. The participation of semiconductor experts from Europe, Japan, Korea, and Taiwan, as well as the U.S.A., ensures that the 1999 ITRS is an even more valid source of guidance for the industry as we strive to extend the historical advancement of semiconductor technology and the worldwide integrated circuit (IC) market. During the past year, those of us involved in the ITRS process have been invigorated by the enthusiasm of our new international partners in this endeavor. Their diverse expertise and dedicated efforts have brought the "Roadmap" to a new level of agreement about future technology requirements for the semiconductor industry. This is a very significant advance toward further fulfilling the goal of the Roadmap to present an industry-wide consensus on the "best current estimate" of our future research and development needs out to a 15-year horizon. As such, it should provide a guide to the efforts of research organizations, and research sponsors within industry, government, and universities.

For four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have been exponential, resulting principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law ("the number of components per chip doubles every 18 months"). The most significant trend for society is in decreasing cost-per-function, which has led to an enormous growth in the market for integrated circuits over the past forty years.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	EXAMPLE
Functionality	nonvolatile memory, smart power
Integration Level	components/chip—Moore's Law
Compactness	components/cm^2
Speed	microprocessor clock MHz
Power	laptop or cell phone battery life
Cost	cost-per-function—historically decreasing at >25% / year

All of these improvement trends have been enabled by significant R&D investments and by industry-wide learning. Within the last two decades, the growing size of the required investments has changed the industry perception of collaboration and "the competitive/pre-competitive boundary." This has spawned many R&D partnerships, consortia, and other cooperative ventures.

TECHNOLOGY REQUIREMENTS PERSPECTIVE

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of microelectronics would further reduce the cost per function (historically, ~25%/year) and promote market growth for integrated circuits (averaging ~15%/year). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for us to stay on Moore's Law and the other trends?" During the 1980s and '90s, this challenge has become so formidable that more and more of the development effort has been shared in a precompetitive environment including consortia and collaboration with suppliers. In this process, the ITRS serves as a guide to the principal technology needs. It does this in two ways: (1) showing the relatively near-term "targets" that need to be met by "technology solutions" currently under development, and (2) indicating where there are no "known solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. This latter situation is highlighted as "red" on the Roadmap. The "red" is officially "on" the Roadmap to clearly warn where progress might end if some real breakthroughs aren't achieved in the future. Such breakthroughs would result in the "red" turning to "yellow" and, ultimately, "white" in future editions and could easily be

responsible for new concepts appearing "on" the Roadmap. In fact, the rate of migration of useful new concepts onto the Roadmap could be used as a measure of its success in fostering technology progress.

For some Roadmap readers, the "red" designation may not have adequately served its purpose of highlighting significant and exciting challenges. There can be a tendency to view any number in the Roadmap as "on the road to sure implementation" regardless of its color. An analysis of "red" usage might classify the "red" parameters into two categories:

(1) where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which we don't have much confidence in any currently proposed solution(s), or

(2) where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end).

A conservative interpretation might view "red" parameters of the "second kind" as effectively "beyond" or "off" the Roadmap. In future editions of the ITRS, we may try to distinguish these cases ("shades of red") or use other means to clarify the often-used but poorly defined terminology "on/off the Roadmap."

Another sense in which items may be "on/off the Roadmap" is in terms of the breadth of technology addressed. The scope of the 1999 ITRS specifically includes detailed technology requirements for all "Complementary Metal-Oxide-Silicon" (CMOS) integrated circuits, including mixed-signal products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound-semiconductor, discrete, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most "thin-film-process-based micro/nanotechnology."

The ITRS time horizon (15 years) provides another boundary to what may be considered "on/off the Roadmap." To date, each edition of the ITRS has been built around a view toward continued scaling of CMOS technology. However, with the 1999 edition, we are reaching the point where the horizon of the Roadmap approximately coincides with the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths of roughly 20 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, future editions of the ITRS may begin pointing toward more radical approaches to perpetuate our ability to further reduce the cost-per-function and increase the performance of integrated circuits. It is probable that such approaches will involve new devices as well as new manufacturing paradigms. It is a strong intent of this edition of the Roadmap to help us prepare for the future by enhancing communication and stimulating creative solutions to the many critical issues and research needs identified herein.

POTENTIAL SOLUTIONS PERSPECTIVE

The ITRS attempts to avoid prematurely identifying definite solutions to the future technology challenges. This is difficult, since guidance on the needs is intended and "one person's need is sometimes another person's solution" (for example, via the customer-supplier relationship or some other type of connection within the "technology hierarchy"). Despite this need to provide guidance, the Roadmap participants are continually pursuing new ways to prevent the Roadmap itself from being interpreted as limiting the range of creative approaches to further advance microelectronics technology. One of the resulting compromises has been to only present illustrative examples of potential solutions to selected challenges in the ITRS. In all cases, it should be noted that these are not to be construed even as complete lists of all solutions suggested to date, much less limits on what should be explored in the near future. A few of the potential technical solutions are listed, where known, just to convey current thinking and efforts. Furthermore, the listing of a particular potential solution does not constitute an endorsement by the Roadmap process. It is *not* the intent of this document to convey or to be interpreted as portraying the most likely solutions to be adopted, nor to focus attention on those potential solutions currently known at the expense of other innovative concepts. In fact, it is eagerly hoped that this Roadmap will inspire additional innovative concepts. The semiconductor industry's future success continues to depend on new ideas.

OVERALL ROADMAP PROCESS AND STRUCTURE

Each technology-area chapter of the ITRS is written by a corresponding International Technology Working Group (ITWG) consisting of experts in that field from industry (chip-makers as well as their equipment and materials suppliers), government, and universities. In addition, each edition of the ITRS incorporates feedback gathered from an even larger community through "sub-TWG meetings" and public "Roadmap Workshops." For this edition, an ITRS Workshop was held on July 8–9, 1999 in Santa Clara, California. The Roadmap resulting from this broad input is, hopefully, a "best-attempt" at building the widest possible consensus on the future technology needs of the semiconductor industry.

The ITWGs are of two types: "Focus" TWGs and "Crosscut" TWGs. The Focus TWGs correspond to typical sub-activities that sequentially span the "Design/Process/Test/Package product flow" for integrated circuits. The Crosscut TWGs represent important supporting activities that tend to individually overlap with the "product flow" at many critical points. For the 1999 ITRS, the Focus TWGs are the following:

- Design
- Test
- Process Integration, Devices, & Structures
- Front-End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly & Packaging

Similarly, the 1999 Crosscut TWGs are the following:

- Environment, Safety, & Health
- Defect Reduction
- Metrology
- Modeling & Simulation

Each ITWG has two representatives from each of the five geographical regions (Europe, Korea, Japan, Taiwan, and the U.S.A.). These representatives are typically elected from "domestic" TWGs in each of their regions. Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which also has two members from each region (for example, representing a regional coordinating committee such as the SIA Roadmap Coordinating Group [RCG] for the U.S.A.).

The principal IRC functions include:

- providing guidance/coordination for the ITWGs,
- hosting the ITRS Workshops, and
- editing the ITRS.

A central part of the IRC guidance/coordination is provided through the up-front creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics (ORTC) Tables. These tables summarize key high-level technology requirements, which define the future "Technology Nodes" and, generally, establish some common reference points for establishing consistency between the chapters written by individual ITWGs. The high-level targets expressed in the ORTC Tables are based, in part, on the compelling economic strategy to maintain the current high rate of advancement in integrated circuit technologies. Thus, the ORTC provide a "top-down business incentive" to balance the tendency for the ITWGs to become conservative in expressing their individual, detailed future requirements.

The "principal tables" in each chapter are individual Technology Requirements tables, patterned after the ORTC Tables. For the 1999 ITRS, the ORTC and Technology Requirements tables have been separated into "Near-Term Years" (1999 through 2005, annually) and "Long-term Years" (2008, 2011, and 2014). This new format is illustrated in Table B, which contains a few key "lithography-related" ORTC lines.

Table B ITRS Table Structure—
Key Lithography-Related Characteristics by Product Type

NEAR-TERM YEARS

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
DRAM ½ PITCH (nm)	180	165	150	130	120	110	100	D ½
MPU GATE LENGTH (nm)	140	120	100	85-90	80	70	65	M GATE
MPU / ASIC ½ PITCH (nm)	230	210	180	160	145	130	115	M & A ½
ASIC GATE LENGTH (nm)	180	165	150	130	120	110	100	A GATE

LONG-TERM YEARS

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
DRAM ½ PITCH (nm)	70	50	35	D ½
MPU GATE LENGTH (nm)	45	30–32	20–22	M GATE
MPU / ASIC ½ PITCH (nm)	80	55	40	M & A ½
ASIC GATE LENGTH (nm)	70	50	35	A GATE

The ORTC and Technology Requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Ideally, the Roadmap might show multiple timing points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is currently estimated. The "default" point is called "Year of Introduction" in the ITRS, which may be characterized as "at the leading-edge of ramp to volume manufacturing." Note, however, that some rows in the ORTC and Technology Requirements tables refer to other timing points, which are defined for each case (e.g., "at sample"). Of course, for the "Long-term Years," it's possible for the "best-estimate year of introduction" to fall in between the selected 3-year table intervals for some technology requirements. However, this will generally not be the case, since the concept of "Technology Nodes" attempts to synchronize technology development around a "synergistic cycle" that has historically been linked to the introduction of new Dynamic Random Access Memory (DRAM) Generations with a 4× increase in bits/chip. For as long as this cycle strictly followed Moore's Law (3-year cycle for 4×), the Technology Nodes and DRAM generations were essentially synonymous. However, in recent years, the "technology-development cycle" has been closer to two years. In addition, a greater diversity of products serving as technology drivers, faster-paced introduction/optimization of product-specific technology, and the general increase in business and technology complexity are all tending to "de-couple the parameters" that have traditionally characterized "advance to the next technology node." For example, it is obvious that the scaling of transistor gate length and copper metal linewidth are relatively independent of the scaling of DRAM cell area. They are all still fundamentally limited by lithography capability, but, today, there are many other very influential factors. In fact, even the choice of basic lithography technology has tended to become more "product specific" (such as "pushing the wavelength as fast as possible" versus "using phase-shift masks"). Thus, for future editions of the ITRS, we will need to revisit the utility of continuing to list "Technology Nodes." However, for 1999, the ITRS shows six nodes of future semiconductor technology, through the "35-nm Generation" (which includes 20–22-nm transistor gate lengths). Thus, note that the "Node Designation" ("35-nm" at the horizon of the 1999 ITRS) is defined by DRAM ½ Pitch (one of the rows in Table B), not by the transistor gate length or minimum feature size characteristic of that Node.

Additional (and, in some cases, more precise) definitions related to the ITRS tables may be found in Appendix B.

TECHNOLOGY DRIVERS

The particular lithography-related rows selected for Table B from the ORTC tables are special in that any one of them may be designated by an ITWG as a "Driver" for any specific row in one of their Technology Requirements Tables. The designation of Drivers for Technology Requirements assists in the process of convergence on the final ITRS tables and also provides an indication of assumed timing dependencies in the final document. Thus, as the Roadmap is updated in subsequent editions, this information will be used for constructing a first-pass strawman version of the new tables. For example, if the requirements in any of these Driver Rows of the ORTC Tables were subsequently pulled-in by one year, it would be assumed that rows in the ITWG Technology Requirements tables would shift by default along with their designated ORTC Driver row. If no Driver is indicated for a particular requirement, there would be no automatic shift; however, interpolation would be used, as necessary to generate new numbers for those rows in columns corresponding to years that were not listed in the previous edition.

TECHNOLOGY NODE CHALLENGES

INTRODUCTION

System-on-a-chip (SoC) devices, for promising use in consumer and industrial electronics applications such as digital communications equipment, have been added to the scope of the *International Technology Roadmap for Semiconductors: 1999*. In addition, DRAM half pitches of 180, 130, 100, 70, 50 and 35 nm have been defined as technology nodes that are general indices of technology development. Each node represents a reduction to approximately 70 percent of the preceding node. Each step represents the creation of significant technology progress.

In addition, specific years have been targeted for the commencement of ramp to mass production (typically, monthly shipments of at least 10,000 units) in each of the various technology nodes. These technology nodes, which are common to all of the Technology Working Groups (TWGs), will facilitate understanding of the Roadmap for the path ahead.

This chapter presents a brief, easy-to-understand summary of the consensus of the Working Groups for each of the technology nodes.

YEAR	*1999*	*2002*	*2005*	*2008*	*2011*	*2014*
TECHNOLOGY NODE (nm)	*180*	*130*	*100*	*70*	*50*	*35*

SYSTEM-ON-A-CHIP

Historically, the Roadmap has emphasized the technological limits of silicon production, leading to the specification of the most complex chips that can be developed in the categories of memory, microprocessor MPU), and ASIC at a particular technology node. With the growing importance of high-volume consumer markets and the ability to integrate almost all aspects of a system design on a single chip, the Roadmap has included an additional vehicle to capture the requirements of this important, emerging area. We refer to this vehicle as a *System-On-a-Chip* (SoC). There are a number of characteristics that distinguish a mainstream SoC, but the main consideration is that it is primarily defined by its performance and cost rather than by technological limits. As a *system*-on-a-chip, these chips are often mixed-technology designs, including such diverse combinations as embedded DRAM, high-performance or low-power logic, analog, RF, and even more esoteric technologies like Micro-ElectroMechanical Systems (MEMS) and optical input/output. In all categories of the Roadmap, design productivity is a key requirement. This is particularly true for the SoC category, where time-to-market for a particular application-specific capability is a key requirement of the

designs. For primarily cost and time-to-market reasons, we expect that product families will be developed around specific SoC architectures and that many of these SoC designs will be customized for their target markets by programming the part (using software, FPGA, Flash, and others). This category of SoC is referred to as a *programmable platform*. The design tools and technologies needed to assemble, verify, and program such embedded SoC's will present a major challenge over the next decade.

DESIGN WORKING GROUP

The advances that enable manufacturing at the aggressive technology nodes of this Roadmap give rise to great challenges in design, verification, and test. Design complexity is increasing superexponentially because of the compounding effects of increased density and number of transistors, increased heterogeneity of design types on a singe chip (such as in SoC designs), and the increasing number of factors that design tools and methods must consider with smaller feature sizes and higher levels of integration. The demands for faster time to market; higher performance digital MPUs and ASICs; mixed-signal and mixed technology designs incorporating analog, RF, MEMS, and others; and parts composed from separately designed IP all produce challenges on various complexity scales. *Silicon complexity* is increased with the much larger numbers of interacting devices and interconnects and the impact of new technologies, new logic families to meet performance goals, and the effects of power and current requirements. *System complexity* is growing not only because of increased system size, but due to SoC designs with a diversity of design styles, integrated passive components, and the increased need to incorporate embedded software. *Design procedure complexity* is also increasing with the growing interaction among design levels, the difficulties of convergence and predictability of the design process, and the growing size and dispersion of design teams—all required for quality, productivity, and time-to-market. *Verification complexity* rises with the need to validate core-based and mixed-technology designs, timing and function together, and behavior at the system level. And the *test complexity* grows greatly at higher speeds, higher levels of integration, and greater design heterogeneity, making external test-through-pins less viable.

TEST WORKING GROUP

The basic requirements are high test reliability (corresponding to low field failure rates) and low test costs. The ability to test for failure modes, such as those associated with the cross-talk caused by high density interconnect, is already essential in nodes above 100 nm. Research in this area must be facilitated. Moreover, testing of embedded mixed analog/digital circuits, and the use of Design-for-Test (DFT) for testing high-speed devices using both low-cost and low-speed testers, present major challenges above 100 nm. Built-In-Self-Test (BIST), which can generate a test pattern and store results within a chip, is a potential solution to both of these problems.

Testing of SoC for nodes below 100 nm is another major issue, and there is a need for the development of a higher-order DFT. Below 100 nm, the potential for the salvage of otherwise unusable chips, using the Built-In-Self-Repair function of memories and logic devices (incorporated in testing processes), will also be explored.

PROCESS INTEGRATION, DEVICES, & STRUCTURES WORKING GROUP

Past trends in DRAM chip size indicate that chip size increased by 1.4× for every four times increase of bit capacity. This progression, if continued further, would make chip sizes too large and lead to problems with the size of lithographic exposure areas and packaging. Accordingly, a model has been proposed in which chip size will now be increased 1.2× for every four times increase of bit capacity. This new model corresponds well with the current trend for a doubling of memory capacity every two years. The deviation from the previous trends in the expansion of memory size, as exemplified by this new model, will necessitate the development of new cell structures, such as open-bit-line cell or cross-point-cell structures, among others, which are characterized by smaller cell sizes relative to the design rules.

For further scaling of MOSFETs, it is necessary to achieve device design for higher performance and minimum variation in product specifications, while effectively addressing the issues associated with gate dielectrics and pn junctions as described in the *Front End Processes* chapter. The introductions of halo doping, as a channel formation technology, and of a high-mobility silicon-germanium epitaxial layer may be

considered potential solutions down to 100 nm. At nodes below 50 nm, the use of novel switching devices, such as quantum-dot or single-electron transistors, may be needed in regions where the statistical variance in the measurements of number and position of impurities becomes significant. New storage devices, such as ferroelectric RAMs (FeRAMs) and MRAMs, which are nonvolatile RAMs, may prove to be viable solutions for memory. For analog and mixed-signal devices, noise problems must be effectively dealt with as the operating voltage becomes lower (2.0–1.5 Volts). At the same time, maintaining capacitor capacity and minimizing parasitic capacitance will be technical challenges upon further scaling of devices. The former problem will be dealt with through adoption of high κ material, while the latter will be effectively resolved by use of low κ dielectrics, copper multi-layer interconnect, SOI substrates, and three-dimensional structures.

In SoC devices with embedded memory, logic, and analog circuits, noise due to interference between different circuit blocks such as digital and analog circuits must be suppressed. In addition, highly integrated processes with excellent cost-performance are required in order to control ever-increasing processing steps and growing chip sizes.

FRONT END PROCESS WORKING GROUP

Technology breakthroughs, in terms of materials and processes, are needed for further scaling because existing materials and technologies are approaching their physical limits. Significant issues include: the use of physically thicker (than silicon dioxide) gate materials to minimize direct tunnel current through the MOSFET gate while maintaining high-capacitance (higher κ); the use of metal gate electrodes to compensate for slower processing speeds caused by depletion in poly-silicon electrodes and boron penetration of the silicon substrate (from the poly-silicon); and methods for forming ultra-thin and low-sheet-resistance pn junctions for higher performance transistors. Moreover, the new materials to be used for gates and dielectrics tend to make the gate etching process more difficult. In addition to CD uniformity and selectivity, etch profiles and line edge roughness must be controlled properly to maintain optimal transistor performance.

Down to the 100 nm node (65 nm gate length), Si_3N_4, unary metal oxides and silicates, with equivalent oxide thickness down to about 1 nm, may be used in MOSFET gate stacks. Raised source/drain, plasma doping and laser annealing methods are candidates for ultra-thin junctions. Additionally, BST may be used as a high κ dielectric for DRAM storage cell scaling, and Ru or RuO_2 may be used for electrodes.

MOSFETs from 65 nm down to 20 nm gate length may require very high κ (>20) gate dielectrics and/or "dual-gate" SOI structures. Vertical MOS may also be used. Open-bit-line cells, cross-point cells and multi-state circuits present good prospects for use as DRAM cell architectures.

Another important breakthrough area is the substrate used in device manufacture. Despite aggressive actions taken to limit chip size, it is generally recognized that at some point in time substrates beyond 300 mm (such as 450 mm) in diameter will need to be introduced in order to manage the manufacturing costs of large chip size devices. The achievement of acceptable cost/performance characteristics of these large substrates constitutes another area where breakthroughs will be needed.

LITHOGRAPHY WORKING GROUP

Scaling must be achieved at reasonable cost and in accordance with the timing technology mentioned above. A 70% reduction from the previous node has typically been achieved within two-three years through shortening of the wavelength of light sources, increased numerical aperture (NA) for optical systems, utilization of half-tone phase-shift masks and other resolution enhancement technologies (RET) such as annular illumination, and the development of high-performance resists. Optical lithography may be extended in the near future through the development of 157 nm technology, which uses F_2 laser light, as well as alternating phase-shift masks and other high-resolution techniques. (Beyond 157 nm, solutions using extreme ultraviolet (EUV), electron projection lithography (EPL), electron-beam direct-write (EBDW), proximity X-ray lithography (PXL) and other "next-generation lithography" (NGL) technologies will have to be developed.) 157 nm light tends to be absorbed by oxygen and organic materials, so there will be a need for oxygen-free exposure equipment, as well as for new resist materials and processes. NGLs generally

employ principles beyond those currently used in "refractive" optical lithography, and innovations will be required in light sources, "optical" systems, masks, resists and almost all other aspects of the technology. Potential solutions at each node are listed below as follows:

NODE	*POTENTIAL SOLUTIONS*
180 nm	KrF
130 nm	KrF+RET, ArF
100 nm	ArF+ RET, F2, EPL, PXL, IPL
70 nm	F2+RET, EPL, EUV, IPL, CBDW
50 nm	EUV, EPL, IPL, CBDW
35 nm	EUV, IPL, EPL, CBDW, Innovative Technology

Mask-making capability and cost escalation have become the major limiter to lithography progress. With the roadmap acceleration over the past three years, the mask industry has fallen behind the requirements of the chipmakers. Mask equipment and process capabilities for complex OPC and PSM are just becoming available for the 180 nm node production requirements. These capabilities are being pushed beyond their limits for 130 nm to 100 nm development. Mask processes for advanced technologies (157 nm, XRL, EUV, EPL, and IPL) are in research and development.

The difficult challenges common to all nodes include controlling critical dimensions, overlays, and defect density. These challenges are not only caused by "relative scaling" but are increasingly related to "absolute sizes," especially at nodes under 100 nm. For example, as actual processing dimensions are getting close to the sizes of photoresist molecules and other physical distances associated with exposure and development, existing techniques for measuring sizes, positions, and defects are becoming difficult to use (as described in detail in the *Metrology* and *Defect Reduction* chapters). In addition, the displacement of the equipment's structural parts due to heat and vibration is no longer negligible.

INTERCONNECT WORKING GROUP

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground to and among the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes. As supply voltage is scaled or reduced, cross-talk has become an issue for all clock and signal wiring levels; the near term solution adopted by the industry is the use of thinner copper metallization to lower line-to-line capacitance. Although copper-containing chips were introduced in 1998, copper must be combined with new insulator materials. The introduction of new low κ dielectrics, CVD metal/barrier/seed layers, and additional elements for SoC, provide significant process and process integration challenges. Interfaces, contamination, adhesion, leakage, and thermal budget, confounded by the number of wiring levels for interconnect, ground planes and other passive elements, create a difficult to manage complexity. Further, although the technical product driver for the smallest feature size remains the dynamic memory chip, an emerging classification of chips, the system-on-a-chip, or SoC, will challenge microprocessors for increased complexity and decreased design rules. Managing this rapid rate of materials introduction and the concomitant complexity represents the overall near term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. New design or technology solutions (such as coplanar waveguides, free space RF, optical interconnect) will be needed to overcome the performance limitations of traditional interconnect.

FACTORY INTEGRATION WORKING GROUP

Factory Integration's basic needs include improved factory productivity through cost reduction; adaptability in the face of change; improved reliability and availability; and shorter production cycle time. In the near term, a focus has been placed on the wafer processing aspect of semiconductor fabrication and on comparisons and contrasts between high-volume/high-mix and high-volume/low-mix production lines. The "management of complexity" is considered to be a fundamental issue that must be further examined. The broad concept of complexity represents the introduction of a wide variety of new products and technologies;

the diversification of processes; the use of large-diameter wafers; and increased reliance on factory automation and systematization. Two subordinate issues, "factory optimization" to reduce costs and shorten production cycle time, and the "flexibility/extendibility" required to accommodate multiple generations of products and larger-scale factory operations, have also been addressed. Factory operations is the umbrella under which the requirements for production cycle time and the operating rates for production lines, among other things, can be examined. Assuming a high-volume/high-mix production line, the required production cycle time, by mask layer, for each of the technology nodes is determined as follows:

TECHNOLOGY NODE (nm)	**180**	**130**	**100**	**70**	**50**	**35**
Non Hot Lot Production Period per Mask Layer (days)	**1.8**	**1.6**	**1.4**	**1.3**	**1.2**	**1.1**
Hot Lot Production Period per Mask Layer (days)	**0.9**	**0.85**	**0.8**	**0.75**	**0.7**	**0.65**

Direct and single-wafer transport with realtime dispatching is needed by the 100 nm node. In addition, for manufacturing equipment, a reduction of non-production (dummy, conditioning, and test) wafers is needed.

ASSEMBLY & PACKAGING WORKING GROUP

The reduction in package size and the effective dissipation of heat are basic needs. In logic chips with 800 pins or higher, the conventional package design (in which terminals are present only on the periphery of the chip) is inappropriate, since the chip area must be increased for installation of the terminals alone. Instead, the area array configuration must be adopted because the package has terminals arranged in grid form on the entire surface of the chip. In order to achieve further reduction in size of packages and high density boards at low cost, flip-chip connection in ball grid arrays (BGAs) is expected to produce good results. Conventional ceramic substrates will have to be replaced with low-cost organic materials for most applications. Required performance characteristics include lower hygroscopy, higher CTE matching to chips, and higher glass transition temperatures, as necessitated by the use of lead-free solder for environmental reasons. Metal lines on the substrate must accommodate much finer-pitch terminals and fan-out wiring. Moreover, improved adhesion and moisture resistance for increased mechanical strength of connections, as well as improved hygroscopy for increased reliability, will be needed for the underfill materials for flip chips. There is also a need for the establishment of superior thermal design and simulation procedures for packages and devices with more effective heat dissipation characteristics and for the development of test methods which provide an assurance of quality and reliability for high-density substrates and semiconductor packages without relying on probes. The development of technologies for the integration of area array/flip chip connections with fine-pitch ball grid arrays (FBGA) / chip-size packages (CSP) is a prerequisite for further reduction, and the use of ultra- fine fan-out wiring will be essential.

ENVIRONMENT, SAFETY, & HEALTH WORKING GROUP

Chemical materials and equipment management includes provision for the dissemination of information concerning the environment, safety, and health to engineers prior to the use of new chemical compounds and materials to prevent problems in these areas following the release of new technologies and products. Efforts to reduce energy consumption in semiconductor production factories and facilities help to eliminate a major cause of global warming and mitigate the factors contributing to climatic change. Worker protection programs are designed to improve existing factories, facilities, safety equipment, training, and education to safeguard the safety and health of workers. Resource conservation programs serve to conserve water, energy, chemical compounds, and materials and other raw materials, and to promote the development of substitutes for toxic materials and the recycling of industrial wastes. Design and management methods will focus on the identification of materials and processes that minimize environmental pressures and the risks to health and safety.

For the nodes of 70 nm or below, the use of new chemical substances in semiconductor fabrication processes is highly likely. There is a need, therefore, for the development of methodologies for the prompt provision of information on environmental effects from a comprehensive examination of any new chemicals. Given the fact that there is increasing societal demand for resource conservation and for effective measures to counter

climatic change, the development of substitute materials with reduced environmental effects and efficient recycling technologies will be essential.

DEFECT REDUCTION WORKING GROUP

The product yield is one of the basic indicators of the completeness of a semiconductor technology. To maintain a high yield, defect reduction is a continuing challenge that is common to all nodes. With progress between nodes, devices will become ever more complex. In reality, the amount of data that must be processed for correct trouble-shooting performance is 80 times higher at the 50 nm node than it is at the 180 nm node. The requirements for defect analysis systems, including defect detection equipment, have become increasingly stringent. This has made defect reduction a far more difficult proposition.

The accuracy of defect inspection equipment for patterned wafers based on conventional technology (ultraviolet light) has already proved inadequate in meeting the requirements for mass production at the 130 nm node. There is no inspection equipment capable of detecting and analyzing defects in high-aspect-ratio circuit patterns. Moreover, the classification speed for defects; the number of defects that can be handled; and the speed of chemical element analysis will also be inadequate; thereby, making it extremely difficult to identify the causes of defects. Accordingly, new defect detection equipment must be developed to satisfy the requirements for lower defect rates.

METROLOGY WORKING GROUP

Even at the 180 nm node, current metrology capability does not meet precision and accuracy requirements for many measurements done during device manufacturing. Aggressive scaling is accelerating the gaps found at the 130 nm node and beyond. The roadmap expresses a strong concern about the gap in capability for sub 100 nm wafer and mask level critical dimension and other inline microscopy measurements. Mask metrology needs are more difficult to meet due to optical proximity correction and phase shift mask structures, and thus they receive an expanded coverage. Future challenges come from the high aspect ratio structures, ultra thin layers, ultra-shallow junctions combined with the use of new materials for transistor, capacitor, and on-chip interconnect. Interfaces between materials require some form of process control. The move toward greater use of measurement data for automated process control and the use of clustered or *in situ* metrology has come to be known as “Integrated Metrology”. There is a need to develop measurement technology for Integrated Metrology. Characterization and metrology for contamination control for the 70 nm node and beyond will be a significant concern.

MODELING & SIMULATION WORKING GROUP

The focus of modeling and simulation is on improvements in the efficiency of development as well as of production. Optimal processes, electrical characteristics, heat damage, and the reliability of devices will be forecast based on theoretical models in order to optimize process/device/circuit designs. In so doing, cost reductions of 25% and 35% may be achieved, respectively, at the 130 nm and 100 nm nodes. In addition to the improvement of existing models, new models for processes in lithography, etching, CVD, and other technologies will have to be developed as scaling progresses down to the 100 nm node. Greater understanding of plasmas, wafer surface reactions, exposure/development of photoresists, and other complex reactions will also be necessary. In addition, improvements in grid (mesh) generation and numerical calculation algorithms will be required to improve calculation speed and accuracy. Below 100 nm, better simulation techniques for newly introduced gate materials, including models of the dielectric constant, the tunneling phenomena and the reliability, must be addressed. In contrast, nanometer devices will have pronounced quantum effects in addition to the obvious effects of discrete atoms in impurities. Thus, precise modeling of the various phenomena observed in processes at the electron level must be established. In contrast to conventional models, which assume the physical continuity of materials, alternative solutions at nodes below 100 nm may include the adoption of discrete modeling procedures: for example, the Monte Carlo methods, in which atoms and electrons are treated as particles, or the quantum dynamic calculation methods, which are based on solving Schroedinger’s equation.

DIFFICULT CHALLENGES TABLES

DESIGN

Table C Design Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Silicon complexity	Large numbers of interacting devices and interconnects Impact of signal integrity, noise, reliability, manufacturability Power and current management; voltage scaling Need for new logic families to meet performance challenges Atomic-scale effects Alternative technologies (such as copper, low κ dielectric, SOI)
System complexity	Embedded software as a key design problem System-on-a-chip design with a diversity of design styles (including analog, mixed-signal, RF, MEMS, electro-optical) Increased system and function size Use of open systems and incorporation into global networks Integrated passive components
Design procedure complexity	Convergence and predictability of design procedure Core-based, IP-reused designs and standards for integration Large, collaborative, multi-skilled, geographically distributed teams Interacting design levels with multiple, complex design constraints Specification and estimation needed at all levels Technology remapping or migration to maintain productivity
Verification and analysis complexity	Formal methods for system-level verification System-on-a-Chip specification Early high-level timing verification Core-based design verification (including analog/mixed-signal) Verification of heterogeneous systems (including mixed-signal, MEMS)
Test/testability complexity	Quality and yield impact due to test equipment limits Test of core-based designs from multiple sources (including analog, RF) Difficulty of at-speed test with increased clock frequencies Signal integrity testability
FIVE ADDITIONAL DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Silicon complexity	Uncertainty due to manufacturing variability Uncertainty in fundamental chip parameters (such as signal skew) Design with novel devices (multi-threshold, 3D layout, SOI) Soft errors
System complexity	Total system integration including new integrated technologies (such as MEMS, electro-optical, electro-chemical, electro-biological) Design techniques for fault tolerance Embedded software and on-chip operating system issues
Design procedure complexity	True one-pass design process supporting incremental and partial design specification Integration of design process with manufacturing to address reliability and yield
Verification and analysis complexity	Physical verification for novel interconnects (optical, RF, 3D) at high frequency Verification for novel devices (nanotube, molecular, chemical)
Test/testability complexity	Dependence on self-test solutions for SoC (RF, analog) System test (including MEMS and electro-optical components)

κ—dielectric constant *SOI—silicon on insulator* *IP—intellectual property*

TEST & TEST EQUIPMENT

Table D Test and Test Equipment Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
BIST and DFT	Test equipment costs will rise toward $20M and wafer yields may suffer without DFT and BIST. DFT required for at-speed test with a low-speed tester. Tools required for inserting DFT and BIST and estimating cost. Analog BIST needed. Access to SoC cores needed when using DFT and BIST.
DUT to ATE interface	A major roadblock will be the need for high-frequency, high pin-count probes and test sockets; research and development is urgently required to lower inductance and cost. Increasing pincounts lead to larger test heads and longer I/O round-trip delays (RTD). This problem can be avoided using two transmission lines, but I/O pins must then drive 25 ohms. Power and thermal management problems Nonuniform wafer temperatures and the requirement for active DUT temperature control Simulation needed for the path from the device through the package to the ATE pin electronics Interface circuits must not degrade ATE accuracy or introduce noise. Especially for high-frequency differential DUT I/O Faster, multi-socket, automatic package handlers are required.
Mixed-signal instruments	IC manufactures must partner with the ATE suppliers to ensure ATE capability will match the mixed-signal requirements These will require more bandwidth, higher sample rates, and lower noise. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits.
Failure analysis	3D CAD and FA systems for isolation of defects in multi-layer metal processes New fault models, such as for crosstalk. Automatic test generators for fault diagnosis. CAD software for fault diagnosis using new fault models to support DFT and BIST requirements.
Test development.	Automatic test program generators to reduce test development time Test standards, such as STIL , IEEE P1500 Reuse of core tests for SoC to reduce test development time Simulation of the ATE, interface, and DUT to avoid test development on expensive ATE. (virtual testing) Data management needs to be integrated into test program development
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
DUT to ATE interface	Optical probing techniques Full wafer test Power and thermal management problems, especially with 300 mm wafers and increasing parallel test sites Contactless probing using BIST (see DFT/BIST section)
SoC test methods	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog BIST Logic BIST for new fault models and failure analysis Deterministic self-test instead of pseudo random test patterns EDA tools for DFT selection considering cost/performance issues
MEMS, sensors, and new IC technologies	Develop new test methods.
New burn-in techniques.	Research is required. Test during burn-in using burn-in DFT/BIST capability; low-cost, massive parallel test during burn-in
Failure analysis.	Realtime analysis of defects in multi-layer metal processes New fault models, such as noise New CAD tools for diagnosis Failure analysis for analog devices

FA—failure analysis
SCAN—A test method in which test patterns are scanned in and out of the DUT.
STIL—IEEE Standard Test Interface Language

PROCESS INTEGRATION, DEVICES, & STRUCTURES

Table E Process Integration, Devices, and Structures Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Meeting device performance targets with available gate stack materials	Production worthy high κ dielectrics and compatible gate materials will not be available.
Function integration at low V_{dd}	Crosstalk, substrate noise, and device performance difficult to optimize simultaneously at high clock rates and low V_{dd}.
Managing power, ground, signal, and clock on multilevel coupled interconnect	Despite the use of low κ dielectrics, interconnect scaling is increasing coupling capacitance, crosstalk and signal integrity issues. Power, clock, and ground distribution will consume an increasing fraction of available interconnect.
Management of increasing reliability risks with the rapid introduction of new technologies.	Inadequate identification and modeling of failure modes in new materials, new operating regions (such as tunneling) and new SoC technologies (such as MEMS)
Integration of precision passive elements	Maintaining high Q, low noise, and tolerances of discrete components.
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
Overcoming fundamental scaling limits for current device structures	Switching drive, noise margin, material properties, and reliability will limit performance improvements from scaling
Integration choices for system-on-a-chip	Cost-effective process integration of many functions on a single chip.
Atomic level fluctuations and statistical process variations	Possible reduction of yield and performance below desired levels due to unacceptable statistical variations.
Design for manufacturability, reliability, and performance.	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, and others
Low-power, low-voltage, high-performance, and reliable nonvolatile memory element	NVM program and erase require voltages that are incompatible with highly scaled low-voltage devices

FRONT END PROCESSES

Table F Front End Process Difficult Challenges

DIFFICULT CHALLENGES THROUGH 2005, LOGIC GATE LENGTH >65 nm	*SUMMARY OF ISSUES*
Nitride Derivatives and High κ Gate Stacks	Effective oxide thickness ~/>1.2 nm for nitride derivatives, ~/< 1.2 nm for high κ Achieve optimal channel mobility >95% of SiO_2 Minimize gate leakage mechanisms to achieve ~/<1A/cm^2 for high-performance logic and ~/<0.001 A/cm^2 for system LSI Control Boron penetration. Minimize gate electrode depletion, e.g., polysilicon depletion Chemical compatibility of dual metal with appropriate work functions
DRAM Storage Cells (Stack and Trench Capacitors)	Implementation of Ta_2O_5, BST, etc., with associated compatible electrode materials Capacitor structures that meet (DRAM ½ Pitch)^2 scaling Trench and stack capacitor scaling to <100 nm
Ultra-Shallow Junctions (USJ) with Standard Processing	Achievement of lateral and depth abruptness Achievement of low series resistance, <10% of channel R_s Annealing technology to achieve ~/<300Ω/□ at ~/<30 nm X_j
L_{eff} Control	Etch CD control and selectivity Sidewall etch control Microloading effects of dense/isolated lines Halo/pocket implant optimization Overall thermal cycle control
Metrology	Physical, electrical and chemical measurement and characterization of gate dielectric, electrodes, USJ, etc.
DIFFICULT CHALLENGES BEYOND 2005 AND AFTER, LOGIC GATE LENGTH ≤65 nm	
Ultra High κ Gate Stack	Effective oxide thickness <0.9 nm Chemical compatibility of dual metal with appropriate work functions Acceptable channel mobility Thermal budget and dielectric stability CD Control Gate Leakage ~/<1A/cm^2 for high performance logic, ~/<0.001 A/cm^2 for system LSI Cost-effective CMOS integration
Memory Storage Cell	Will an alternate storage cell supplant conventional memory? Ultra high κ capacitor dielectric (Epi BST) Are trench and stack capacitor structures viable at or below 70 nm while meeting (DRAM ½ Pitch)^2 scaling?
Alternate and Ultra-scaled Transistor Structures	CMOS structure: raised S/D, replacement gate process flow, CD control, CMOS integration, and others New device structures beyond planar CMOS: pillar, wraparound gate, and others.
Integration of Silicon Compatible Materials	CoO of large wafers (>300 mm): epi, SOI, Si:Ge Development of compatible high κ dielectric materials Development of compatible dual metal electrodes Development of material compatible cleaning processes
Metrology	Physical, chemical and electrical measurement and characterization of new dielectric, electrodes, and ultra-shallow, ultra-abrupt, dopant distributions

LITHOGRAPHY

Table G Lithography Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm THROUGH 2005	*SUMMARY OF ISSUES*
Optical mask fabrication with resolution enhancement techniques for ≤ 130 nm and post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157 nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market
Lithography technology consensus (193 nm + RET, 157 nm, NGL)	Narrowing of Roadmap options for 100–50 nm nodes. Achieving global consensus among technology developers and chip manufacturers
Cost control and return on investment (ROI)	Achieving constant/improved throughput with larger wafers Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, such as low costs masks. Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 7 nm, 3 sigma
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option
FIVE DIFFICULT CHALLENGES < 100 nm BEYOND 2005	
Mask fabrication and process control	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (such as 157 nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm nodes
Metrology and defect inspection	R&D for critical dimension and overlay metrology, and patterned wafer defect inspection for defects < 40 nm
Cost control and return on investment (ROI)	Development of innovative technologies, tools, and materials to maintain historic productivity improvements Achieving constant/improved throughput with post-optical technologies Achieving ROI for industry (chipmakers, equipment and material suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100 nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 5 nm, 3 sigma, and reducing line edge roughness
Overlay improvements and measurements	Development of new and improved alignment and overlay control methods independent of technology option

INTERCONNECT

Table H Interconnect Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
New materials	Rapid introduction of materials/processes are necessary to meet resistivity and low/high κ targets and address SoC needs.
Reliability	New materials create new chip reliability (electrical, thermal and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Process integration	Combinations of materials (Cu, Al, low κ, high κ, ferroelectrics, new barriers/nucleation layers) along with multiple technologies used in SoC applications open new integration challenges.
Dimensional control	Multi-dimensional control of interconnect features is necessary for circuit performance and reliability. Multiple levels, new materials, reduced feature size and pattern dependent processes create this challenge.
Interconnect process with low/no device impact	As feature sizes shrink, interconnect processes must be compatible with device roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.
FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
Dimensional control and metrology	Multi-dimensional control and metrology of interconnect features is necessary for circuit performance and reliability.
Aspect ratios for fill and etch	As features shrink, etching and filling high aspect ratio structures will be challenging, especially for DRAM. Dual damascene metal structures are also expected to be difficult.
New materials and size effects	Continued introductions of materials/processes are expected. Microstructural and quantum effects become important.
Solutions beyond copper and low κ	Material innovation with traditional scaling will no longer satisfy performance requirements. Accelerated design, packaging and unconventional interconnect innovation will be needed.
Process integration	Combinations of materials along with multiple technologies used in SoC applications are a continued challenge. Plasma damage, contamination and thermal budgets are key concerns.

FACTORY INTEGRATION

Table I Factory Integration Difficult Challenges

DIFFICULT CHALLENGES	*SUMMARY OF ISSUES*
Complexity Management	Rapidly changing business needs and globalization trends • Increasing rate of new product and technology introductions • Globally disparate factories run as single "virtual factory" • Need to meet regulations in different geographical areas Increasing process and product complexity • Explosive growth of data collection/analysis requirements • Increasing number of processing steps • Multiple lots in a carrier Larger wafers and carriers driving ergonomic solutions • Increasing expectations for material handling automation systems Increased reliance on factory systems • Multiple system interdependencies • Co-existence of new factory systems with existing (legacy) systems
Factory Optimization	Meet customer ontime delivery • Balanced throughput and cycle time • Reduce time to ramp factories, products, and processes Improve Overall Factory Effectiveness (OFE) • Improve all Factory Integration thrust areas Improve factory yield • Control production equipment and factory processes to reduce parametric variation Reduce product and operation cost • Minimize waste and scrap and reduce the number of nonproduct wafers Satisfy all local, state and federal regulations.
Extendibility, Flexibility, and Scalability	Reuse of building, production and support equipment, and factory systems • Across multiple technology nodes • Across a wafer size conversion Factory designs that support rapid process and technology changes and retrofits • Understand up-front costs to incorporate EFS • Determine which EFS features to include and not to include • Minimize downtime to on-going operations Increase tighter ESH/Code requirements Increase purity requirements for process and materials

ASSEMBLY & PACKAGING

Table J Assembly & Packaging Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Improved organic substrates for high I/O area array flip chip	T_g compatible with Pb free solder processing ε_r approaching 2.0 Improved area array escape wireability at low cost Lower CTE approaching 6.0 ppm/°C Low moisture absorption High density substrate test
Improved underfills for high I/O area array flip chip Reliability limits of flip chip on organic substrates	Improved manufacturability (fast dispense/cure), better interface adhesion, lower moisture absorption, flow for dense bump pitch Reliability up to 170°C for automotive Comprehensive parametric knowledge of packaging components (chip size, underfill, substrate, heat sink, UBM/bump)
Coordinated design tools and simulators to address chip, package, and substrate complexity	Physical design Thermal/thermo-mechanical Electrical (power disturbs, EMI, signal integrity associated w/higher frequency/current, lower voltage, mixed-signal co-design) Commercial EDA supplier support
System reliability impact of Cu/low κ on packaging	Bump and underfill technology to assure low κ dielectric integrity Mechanical strength of dielectrics Interfacial adhesion
Cost effective cooling for cost-performance and high-performance sectors	Meeting 40°C above ambient temperature Localized on-chip power density
DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Close the gap between the substrate technology and the chip	Low-loss, low ε_r materials Cost/unit area constant (cost/layer decreasing) Interconnect density scaled to silicon System level solution that optimizes reliability and cost
"System level" view of integrated chip, package, and substrate needs	Commercial EDA supplier support
Ultra high frequency design for high density digital and mixed-signal packaging	Efficient design and simulation tools Integrated analog to digital design tools
Manufacturability and reliability of large body packages	Substrate flatness Co-planarity of chip-to-package and package-to-board

CTE—coefficient of thermal expansion
EMI—electromagnetic interference
UBM—under bump metallurgy
EDA—electronic design automation

ENVIRONMENT, SAFETY, AND HEALTH

Table K Environment, Safety, and Health Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Chemicals, Materials and Equipment Management	*Chemical Data Collection* Need to document and make available environment, safety, and health characteristics of chemicals. *New Chemical Assessment* Need for quality rapid assessment methodologies to ensure that new chemicals can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation. *Environment Management* Need to develop effective management systems to address issues related to disposal of equipment, and hazardous and non-hazardous residue from the manufacturing process.
Climate Change Mitigation	*Reduce Energy Use Of Process Equipment* Need to design energy efficient larger wafer size processing equipment. *Reduce Energy Use Of The Manufacturing Facility* Need to design energy efficient facilities to offset the increasing energy requirements of higher class clean rooms. *Reduce High Global Warming Potential (GWP) Chemicals Emission* Need ongoing improvement in methods that will result in emissions reduction from GWP chemicals.
Workplace Protection	*Equipment Safety* Need to design ergonomically correct and safe equipment. *Chemical Exposure Protection* Increase knowledge base on health and safety characteristics of chemicals and materials used in the manufacturing and maintenance processes, and of the process byproducts; and implement safeguards to protect the users of the equipment and facility.
Resource Conservation	*Reduce Water, Chemicals And Materials Use* Requirements for large amounts of water, chemicals, and materials limit sustainable growth. *Waste Recycle* Increase in resource use as the result of increasing process complexity will require that efficient waste recycling methods be developed.
ESH Design and Measurement Methods	*Evaluate and Quantify ESH Impact* Need integrated way to evaluate and quantify ESH impact of process, chemicals, and process equipment, and to make ESH a design parameter in development procedures for new equipment and processes.
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Chemicals, Materials and Equipment Management	*Chemical Use Information* Rapid introduction of chemicals and materials into new process requires the understanding of process fundamentals in order to reduce ESH impacts.
Climate Change Mitigation	*Reduce Energy Use* The importance of reducing energy use for climate change will grow. *Reduce High GWP Chemicals Emissions* No known alternatives and international regulatory pressure to reduce emissions of GWP chemicals.
Workplace Protection	*Equipment Safety* Need ergonomic principles integrated into the processing and wafer moving equipment for both operation and maintenance aspects, and into the overall manufacturing facility.
Resource Conservation	*Reduce Water, Energy, Chemicals And Materials Use* Need resource efficient processing and facility support equipment and improved water reclaim and recycling methods. Emphasis on resource sustainability will grow.
ESH Design and Measurement Methods	*Evaluate and Quantify ESH Impact* Need integrated ESH design in development of new equipment and processes.

DEFECT REDUCTION

Table L Defect Reduction Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Yield Models—Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process induced defects, equipment generated particles and product/process measurements to yield	Correlated process-induced defects (PID), particles per wafer per pass (PWP), product inspections, and *in situ* measurements Sampling and statistical issues with ultra-small populations Impact of within-wafer variations on yield predictions Development of parametric yield loss models
High Aspect Ratio Inspection—High-speed, cost-effective tools must be developed that rapidly detect defects associated with high-aspect ratio contacts/ vias/trenches, and especially defects near/at the bottom of these features.	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Trace Impurity Specifications—Test structures and advanced modeling are needed to determine the effect of trace impurities on device performance, reliability and yield.	The need to better understand the impact of trace impurities is expected to become more important as new materials and processes are introduced.
Defect Sourcing—Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions.	Circuit complexity grows exponentially and the ability to rapidly isolate failures on non-arrayed chips is needed. Automated data reduction algorithms must be developed to source defects from multiple data sources (facility, design, process and test.)
Nonvisual Defects—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.	Many defects that cause electrical faults are not detectable inline.
FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Yield Models—Defect "budgeting" must comprehend greater parametric sensitivities, complex integration issues, greater transistor packing, ultra-thin film integrity, etc.	Development of test structures for new technology nodes Modeling complex integration issues Ultra-thin film integrity modeling Better methods of scaling front end process complexity that considers increased transistor packing density
Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughputs	Existing techniques tradeoff throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size do may not exist
Escalating Inspection Costs—Equipment must effectively utilize realtime process and contamination control through integrated *in situ* process and product metrology	Equipment must effectively utilize real time process and contamination control through *in situ* sensors. Inspection must occur during yield ramp and by exception only in a production environment.
Defect Characterization—Defect data must include size, shape, composition, location all independent of "background," for accelerated yield learning	Defect characteristic data will be necessary to enable continued yield learning. Inline defect detection data must include size, shape, composition, and so on., all independent of location and topology. Test structures will have to be developed that emulate design to process and process integration issues.
Defect Free Intelligent Equipment—Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation.	Advanced modeling (chemistry/contamination), materials technology, software and sensors are required to provide robust, defect-free process tools that predict failures/faults and automatically initiate corrective actions prior to defect formation Development of advanced low defect surface preparation techniques

METROLOGY

Table M Metrology Difficult Challenges

FIVE DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
Factory level and company wide metrology integration for *in situ* and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species/energy/dosage (current), and wafer temperature during RTA.
Impurity detection (particles, oxygen, and metallics) at levels of interest for starting materials and reduced edge exclusion for metrology tools	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Detectivity of trace metals in bulk silicon or in the top silicon layer of SOI (silicon on insulator) must be enhanced.
Measurement of the frequency-dependent dielectric constant of low κ interconnect materials at 5×to 10× base frequency.	Equipment, procedures, and test structures need to be reduced to practice and applied to low κ interconnect materials that account for clock harmonics, skin effects, cross-talk, and anisotropy of materials.
Control of high-aspect ratio technologies such as damascene challenges all metrology methods.	New process control needs are not yet established. For example, 3-dimensional (CD and depth) measurements will be required for trench structures in new, low κ dielectrics.
Measurement of complex material stacks	Reference materials and standard measurement methodology for new, high κ gate and capacitor dielectrics with interface layers, thin films such as interconnect barrier and low κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers.
ADDITIONAL DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for side wall shape. CD for damascene process may require measurement of trench structures.
Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.	The wearout mechanism for new, high κ gate and capacitor dielectric materials is unknown.
Statistical limits of sub-70 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
3D dopant profiling	The dimensions of the active area approach the spacing between dopant atoms, complicating both process simulation and metrology. Elemental measurement of the dopant concentration at the requested spatial resolution is not possible.
Production worthy, physical inline metrology for transistor processes that provides SPC required to achieve consistent electrical properties	Presently, the combined physical metrology for gate dielectric, CD, and dopant dose and profile is not adequate for sub-70 nm design rules.

SPC—statistical process control

MODELING & SIMULATION

Table N Modeling and Simulation Difficult Challenges

DIFFICULT CHALLENGES ≥100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters (such as from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B); metastable states Implant damage, amorphization, re-crystallization
Unified package/die-level models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Model thin film and etch variation across chip/wafer (Equipment/topography)	Reaction paths and rate constants; reduced models for complex chemistry Plasma models; linked equipment/feature models CMP (full wafer and chip level) Pattern dependent effects
Model alternative lithography technologies	Resolution enhancement; mask synthesis (OPC, PSM) Predictive resist models 248 versus 193 versus 157 evaluation and tradeoffs Next-generation lithography system models
Reliability models for circuit design and technology development	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability, SER, ESD, latch-up
Model new interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy, low κ dielectric materials
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (such as metal) Model epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Accurate atomic scale models for process integration