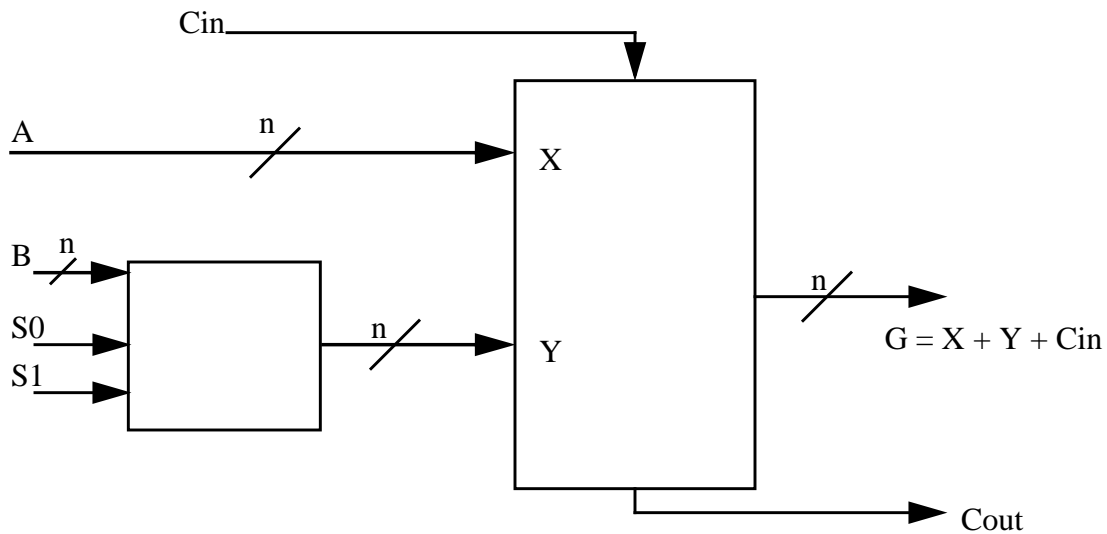# LAB Assignment #6 for CMPE 413/CMSC 711

Assigned: Fri, Oct 20th
Due: Fri, Nov. 2nd

Description: Design and Test a simple 8 function 4-bit two's complement ALU written in VHDL and tested with NC-VHDL.

This is a simple exercise in which you will write a VHDL program which describes an arithmetic unit and you will be required to validate it using the nc simulator.

Select		Input	$G = X + Y + In$	
S_1	S_0	Y	$C_{in} = 0$	$C_{in} = 1$
0	0	all 0's	$G = A$ (transfer)	$G = A + 1$ (increment)
0	1	B	$G = A + B$ (add)	$G = A + B + 1$
1	0	$\overline{B}$	$G = A + \overline{B}$	$G = A + \overline{B} + 1$
1	1	all 1's	$G = A - 1$ (decrement)	$G = A$ (transfer)

Report Requirements:

1) E-mail the VHDL source code as an attachment to the TA at cpatel2@cs.umbc.edu. The subject should be 711 Lab6.

2) Describe the simulation procedure in brief.

3) Turn in the output showing that the ALU implements the functions required. This will require an input file and the corresponding output file. Explain which bits corresponds to which input in the input file and which bits in the output file correspond to which outputs.

4) You must use hierarchy in your design specification. In other words, specifying the entire design as one entity/architecture will earn 0 points. Your write-up should include a diagram that shows which entity calls other entities and what functions each entity performs. An example diagram is shown below.
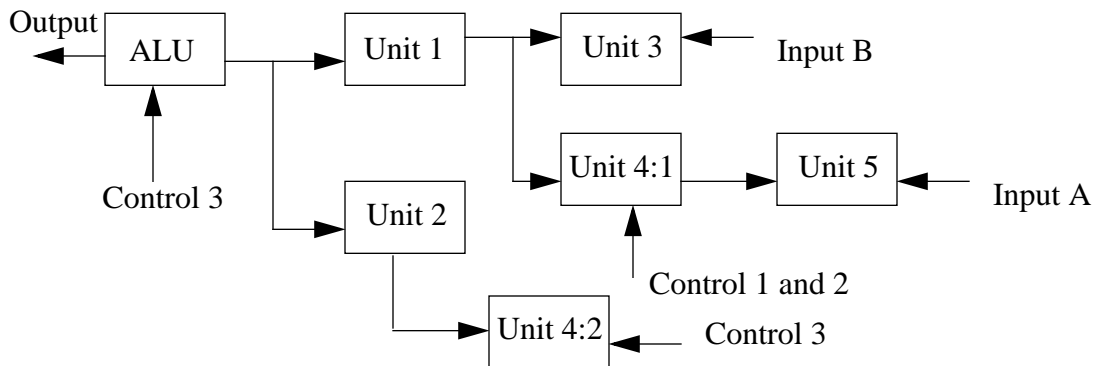
Unit 1 :- Inverts A
Unit 2 :- Modifies A depending on control signal 1 and 2
Unit 3 :- Takes input B and performs 2's compliment
Unit 4 :1 : - and so on.

This is just an example and your design doesn't have to look the same.

5) The major portion of your grades will depend on the correctness of your code. The TA will run a set of tests on your design. In order to make your design file compatible with his test file, you MUST use the following top-level entity and architecture statements EXACTLY as shown below. The ellipses indicate that you must complete that part of the port specification on your own. Failing to follow these instructions will have significant impact on your grade.

```
entity alu_4 is
port (A : ....
      B : ....
      Cin : ....
      S0 : .....
      S1 : .....
      G : .....
      Cout : .......
      );
end alu_4;

architecture structural of alu_4 is
....
....
....
end structural;
```