ITRS

International Technology Roadmap for Semiconductors

The unique factor that has made the semiconductor industry successful:

"Decreases in feature size have provided improved functionality at a reduced cost".

Traditional scaling to **Equivalent scaling**:

Traditional scaling is starting to be effected by fundamental limits of the materials constituting the building blocks of the planar CMOS process.

- Extending the limit will be achieved through the assimilation of new materials for next 5-10 years.
- New devices needed in 10-15 years (alternative to planar CMOS).

Performance improvements of **2x** every **2** years will be difficult to maintain.

Need innovations in circuit and system design, particularly for Performance System-on-a-Chip (**P-SoC**):

- Integration of multiple silicon technologies on same chip.
- Closer integration of package and silicon technology.

ITRS

Feature scaling enables improvements to the following trends:

Trend	Example
Functionality	Nonvolatile memory
Integration Level	Components/chip (Moore's Law)
Compactness	Components/cm^2
Speed	Microprocessor clock
Power	Laptop or cell phone battery life
Cost	Cost-per-function (decreases at >25%/year.

Most of these trends have been exponential.

DRAM 1/2 pitches of six roadmap "technology nodes":

Year	1999	2002	2005	2008	2011	2014
Tech node	180	130	100	70	50	35

Each node is approximately 70% of the previous node.

System-on-a-Chip (SoC):

Often *mixed-technology* designs incorporating:

- Embedded DRAM
- High-performance or low-power logic
- Analog components
- RF components
- Plus possibly Micro-ElectroMechanical Systems (**MEMS**) and optical input/output.

For cost and time-to-market reasons, specific “programmable” SoC architectures will emerge and products will be developed from them.

Software, FPGAs, Flash, etc. will be used to configure these programmable platforms.

Hot research topics:

Design tools are needed to assemble, verify and program them.

Design and Test Complexity Issues

Design complexity is increasing super-exponentially:

- Increased density.
- Increased number of transistors.
- Increased design heterogeneity (SoC).
- Increasing number of factors that design tools and methods must consider with smaller feature sizes and higher levels of integration.

Design and test complexity issues:

- **Silicon complexity** increased:
  With larger number of interacting devices and interconnects.
  With impact of new technologies.
  With impact of new logic families to meet performance goals.
  With effects of power and current requirements.
- **System complexity** increased:
  With increased system size.
  Diversity of SoC design styles, integrated passive components and embedded software.

Design and Test Complexity Issues

Design and test complexity issues (cont.):

- **Design procedure complexity** increased:
  - With growing interaction between design levels.
  - With difficulties in the predictability of the design process.
  - With increases in size and dispersion of design teams.

- **Verification complexity** increased:
  - With need to validate core-based and mixed-technology designs, timing and function together.
  - With the need to validate behavior at the system level.

- **Test complexity** increased:
  - With higher speeds.
  - With higher levels of integration.
  - With greater design heterogeneity.
  - With reduced external access (*test-through-pins* less viable).

Test Issues

Basic requirements:

- High test reliability

  Lower yield loss and field failure rates (higher device quality).
- Low test costs.

New test requirements needed now (for technology > 100nm):

- The ability to test for new failure modes, such as cross-talk induced failures caused by high density interconnect.
- Testing embedded mixed analog/digital circuits.
- Use of *Design-for-Test* (DFT) for testing high-speed devices using both low-cost and low-speed testers.

BIST offers potential solution for the latter two problems.

Process Integration Issues:

Further scaling of MOSFETs for higher performance and minimum variation in product specification may require:

For technologies > 100nm:

- *Halo doping* (as a channel formation technology).
- *High-mobility silicon-germanium epitaxial layer*.

For technologies < 50nm:

- Novel switching devices such as *quantum-dot* or *single-electron* transistors.
- New storage devices such as *ferroelectric RAMs* (FeRAMs) and MRAMs.

For analog and mixed-signal devices, **noise problems** must be addressed for V_{DD}s of 2.0-1.5V.

Process Integration Issues:

Other challenges include:

- Building high capacitance structures
  - Solution: high dielectric materials.

- Minimizing parasitic capacitance:
  - Solutions:
  - Low dielectric materials.
  - Copper interconnect.
  - SOI substrates.
  - 3-dimensional structures.

For SoC:

Mixing embedded memory, logic and analog circuit creates noise problems that must be dealt with.

Processes that support the large number of steps for mixed technology and provide excellent cost-performance are needed.

Process Integration Issues: