entity_declaration:==

entity *entity_name* **is port**

[(port_list)]

end [*entity_name*] ;

port_list :==

{ *signal_name* {, *signal_name* } :

direction signal_type ; }

signal_name {, *signal_name* } :

direction signal_type

direction :== **out** | **in**

signal_type :== **bit_vector** | **bit**

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architecture declaration:==

architecture *architecture_name* **of**
entity_name **is**
{ architecture_declarative_item }
begin
{ concurrent_statement }
end [*architecture_name*] ;

architecture_declarative_item :==

signal_declaration
| component_declaration
| configuration_specification
| label_declaration

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label_declaration :==

label *label_name* { , *label_name* } ;

signal_declaration:==

signal *signal_name* { , *signal_name* }
: signal_type ;

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component_declaration :==

component *component_name*

[**port** (port_list)]

end component ;

configuration_specification :==

for *instantiation_label*

{, *instantiation_label* } :

component_name **use entity**

entity_name(architecture_name) ;

component_instantiation_statement :==

instantiation_label : component_name

port map

([*signal_name* {, *signal_name* }]) ;

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concurrent_statement :==

    concurrent_signal_assignment_statement

    | component_instantiation_statement

concurrent_signal_assignment_statement :==

    [*label_name*:]

        conditional_signal_assignment ;

conditional_signal_assignment :==

    target_name <=

        { *expression* **when** *condition* **else** }

        expression

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Operators

AND	logical and (multiple input)
OR	logical or (multiple input)
XOR	logical xor (multiple input)
NAND	logical nand (two input)
NOR	logical nor (two input)
&	bit concatenation

Key

italics_text	VHDL identifier
bold_text	VHDL reserved word
[. . .]	optional
{. . .}	text repeated zero or more times
|	separates a group of choices

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