Master Slave

```
entity MS is
 port (clear,reset,set,clock:in bit;
       q, qbar: out bit);
end MS;

architecture ms_struct of MS is
signal clrbar, r0, s0, q0, qbar0,
       r1, s1, cbar: bit;
 label rs0, rs1;
 component rs_ff
  port (r,s: in bit;q,qbar: out bit);
 end component;
 for rs0, rs1: rs_ff
 use entity RS(nor_logic);
begin
 clrbar <= not clear;
 cbar <= not clock;
 r0 <= (reset and clock) or clear;
 s0 <= (set and clock) and clrbar;
 rs0:rs_ff port map(r0,s0,q0,qbar0);
 r1 <= (qbar0 and cbar) or clear;
 s1 <= (q0 and cbar) and clrbar;
 rs1:rs_ff port map(r1,s1,q,qbar);
end ms_struct;
```