The Components

```
architecture logic of adder is
-- missing (you saw it before)


end logic;

architecture edge of D_FF is

-- an 8 bit wide edge triggered D FF

 signal x, y, z, w, qb, e :
          bit_vector(7 downto 0);
begin
 e <= "11111111" when enable else 0;
 x <=    din nand y;
 y <=    e nand (not w);
 z <=    e nand w;
 w <=    z nand x;
 dout <= z nand qb;
 qb <=   y nand dout;
end edge;
```