The Declarations

```
architecture mult of multiply is
 signal mux1, mux2, mux3, mux4:
     bit_vector(7 downto 0);
 signal control, adder_out:
     bit_vector(7 downto 0);
 signal accum:
     bit_vector(15 downto 0);
 signal carry_out  :bit;

 label l1, l2, l3, l4;

 component add
  port (arg1, arg2: in bitvec;
          c_in :in bit;
          result :out bitvec;
          c_out :out bit);
 end component;
 for l4: add use entity adder(logic);

 component latch
  port (xin :in bitvec;
   xout :out bitvec; enable :in bit);
 end component;
 for l1, l2, l3: latch use
     entity D_FF(edge);
```