Example Components

```
entity Dlatch is
 port (clk,d: in bit; q,qb: out bit);
end Dlatch;

architecture test of Dlatch is
 --
 signal db, cr, cs: bit;
 --
 component rs_ff
  port (r, s: in bit;
        q, qb: out bit);
 end component;
 --
 label rs0;
 --
 for rs0: rs_ff
    use entity rs(nor_logic);

begin
  db <= not d;
  cr <= db and clk;
  cs <= d and clk;
  rs0: rs_ff port map(cr, cs, q, qb);
end test;
```