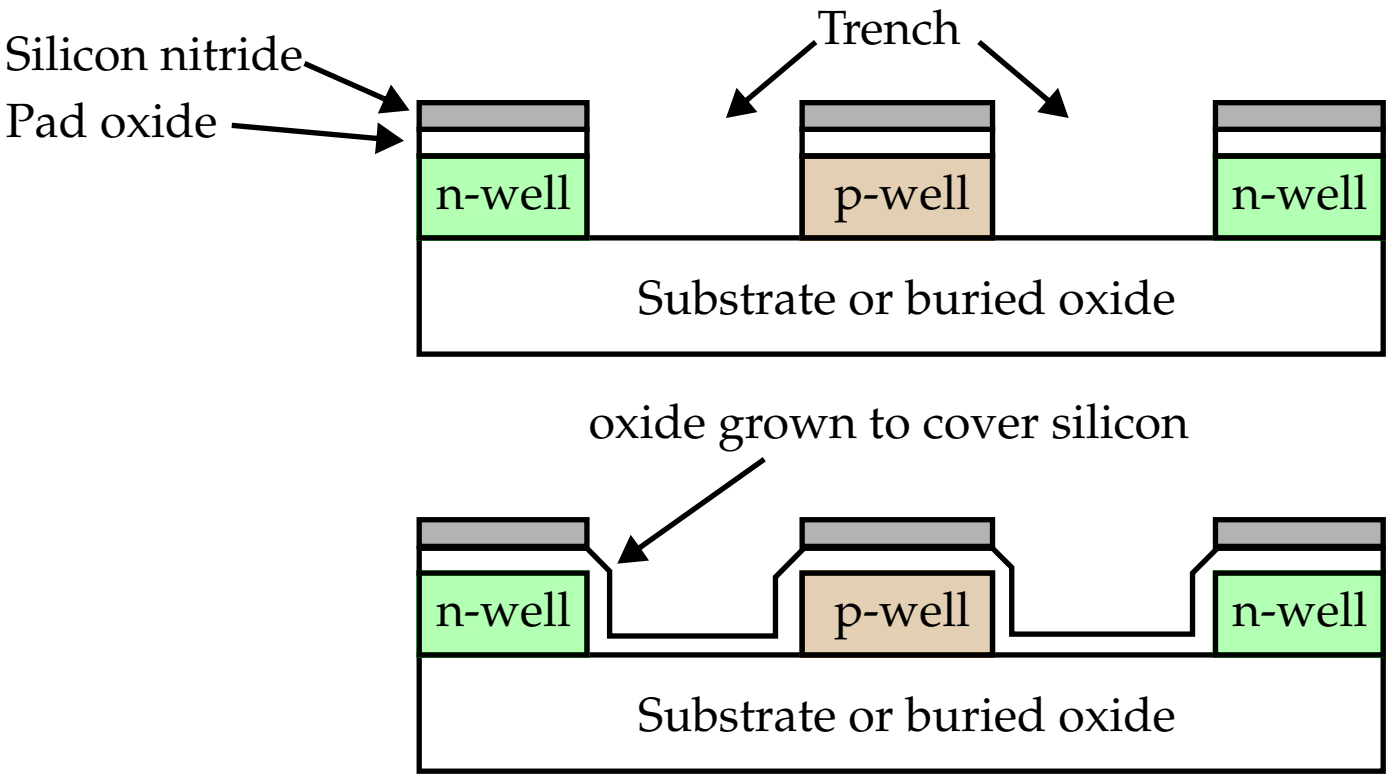
CMOS Processing Technology

Isolation of transistors, i.e., their source and drains, from other transistors is needed to reduce electrical interactions between them.

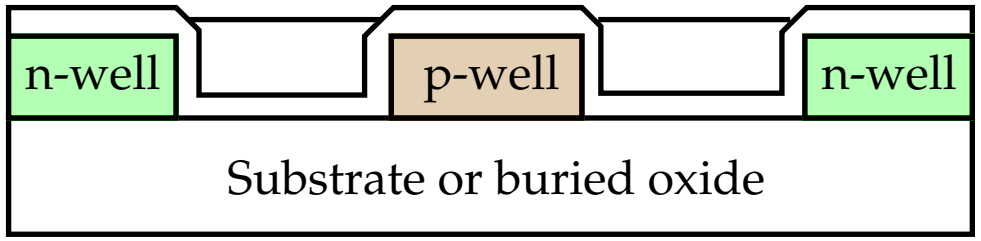
For technologies <180 nm, a process called *shallow trench isolation* (STI) can provide SiO_2 trenches that are 140 nm wide and 400 nm deep.

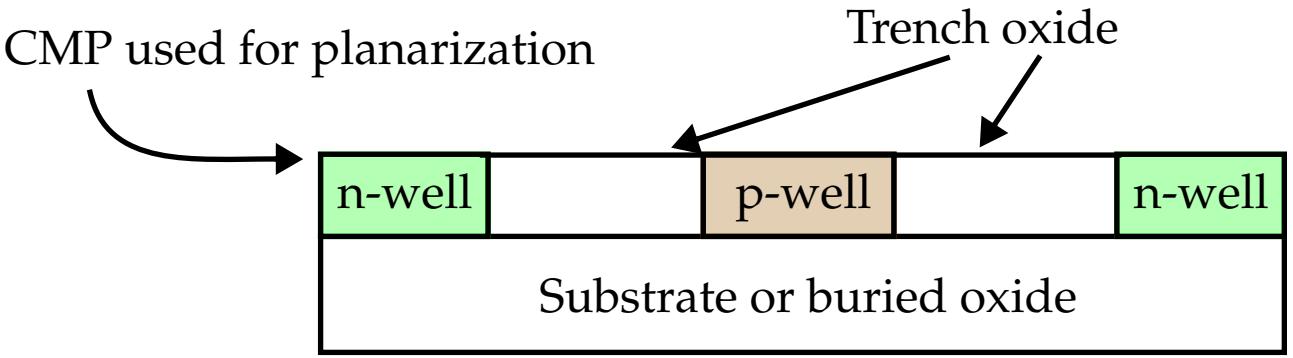
Good for isolation of analog or memory sections from digital sections.



CMOS Processing Technology

Trenches are filled using CVD (does not consume underlying silicon).



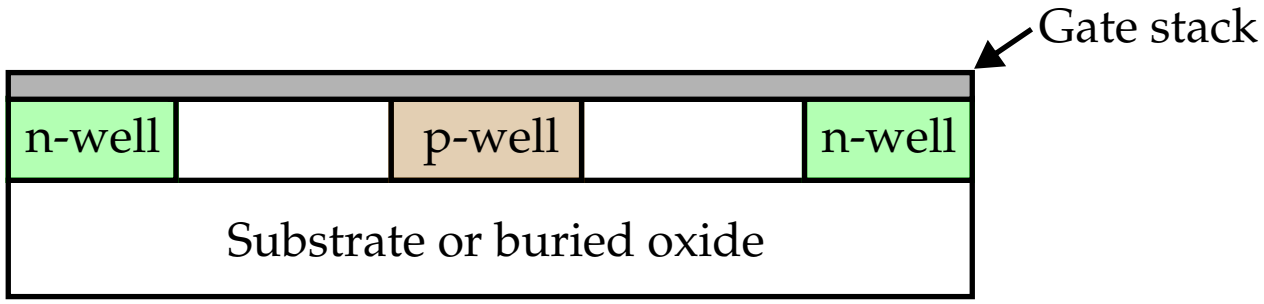


The process also allows for the closer packing of nMOS and pMOS transistors.

It increases the breakdown voltage of the junctions.

CMOS Processing Technology

On top of this planarized surface is grown a gate stack.



Modern processes overlay consecutive layers of SiO_2 followed by *oxynitrided* oxide (nitrogen added).

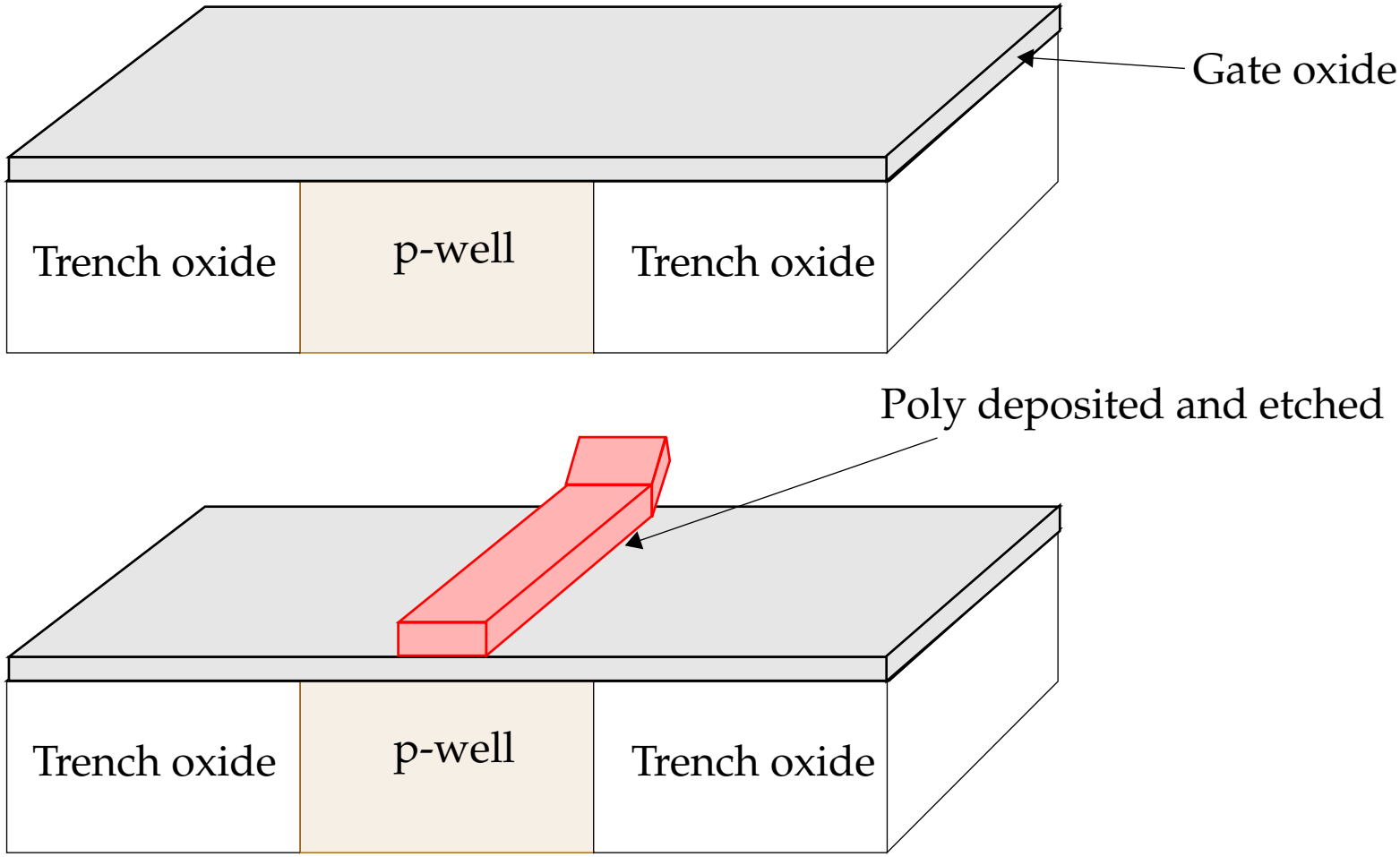
Nitrogen increases the dielectric constant, decreasing the *effective oxide thickness* (for a given oxide thickness, it performs like a thinner layer).

Advanced processes give the designer several oxide thickness options, that trade off performance and gate leakage current.

At the 65 nm node, the effective thickness is on order of 1.5 nm!

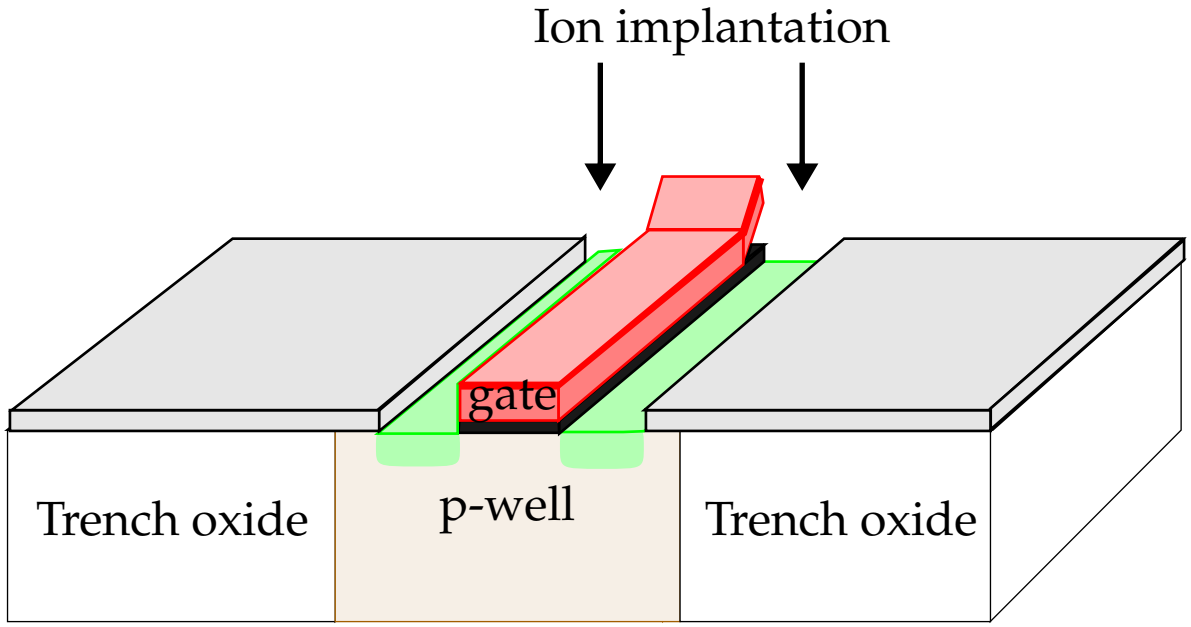
CMOS Processing Technology

Self-aligned polysilicon gate process: Poly acts as a mask for the precise alignment of the source and drain with the gate.



CMOS Processing Technology

Ion implantation is used to create the source and drain regions.



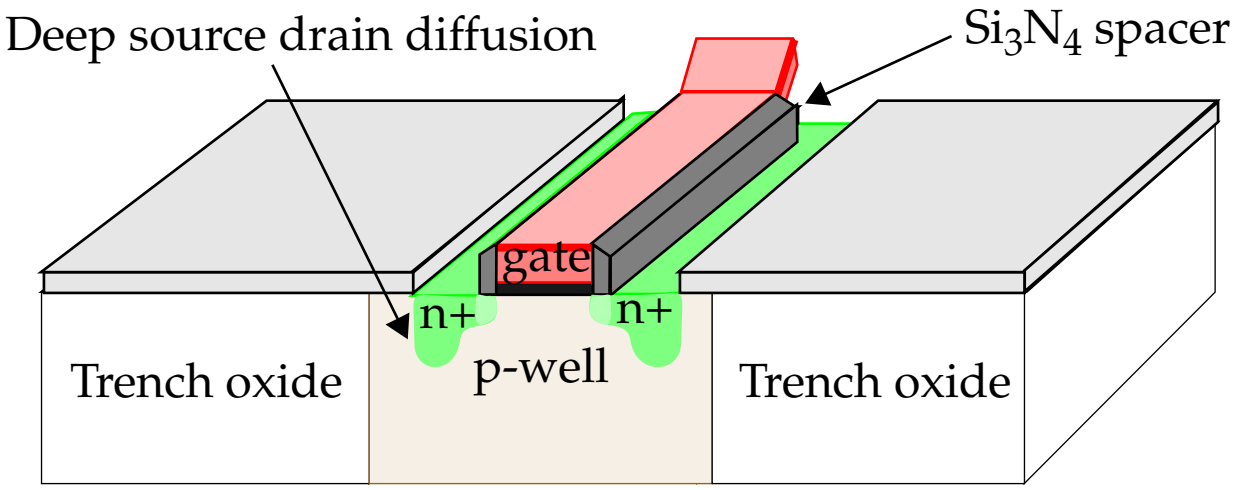
The source and drain implant concentration are relatively low (*lightly doped drain* or LDD), which reduces the electric field at the drain junction.

This improves the immunity of the transistor to **hot electron** damage.

Light doping *decreases* capacitance but *increases* resistance.

CMOS Processing Technology

In order to reduce resistance, a *silicon nitride* spacer is added that acts as a mask to impant a deeper level of diffusion.



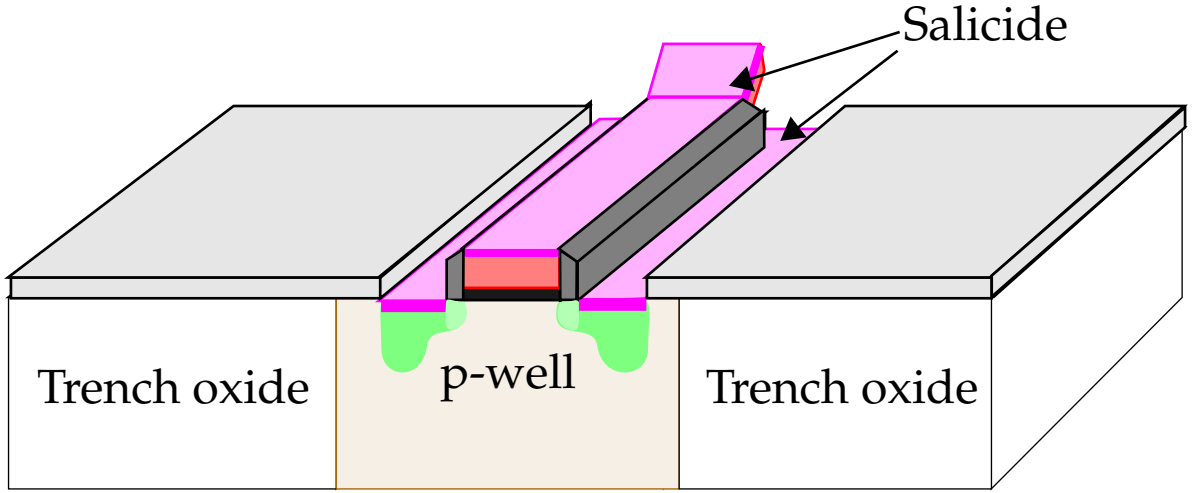
The resistance of the gate, source and drain regions are reduced by introducing a *refractory metal*.

Tantalum, molybdenum, titanium or cobalt.

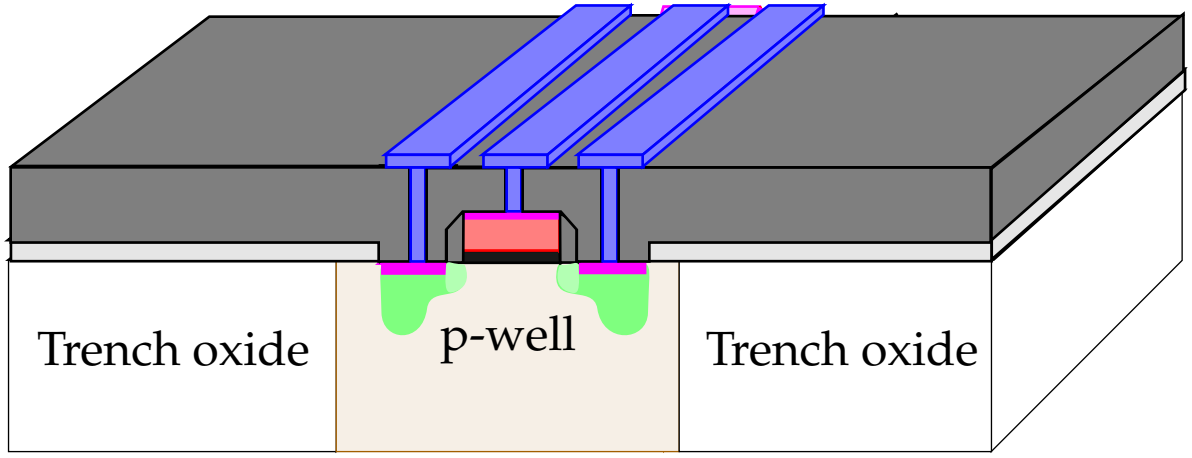
Polyside: Only the gate is silicide.
Salicide: Gate, source and drain are silicide.

CMOS Processing Technology

Self-aligned silicide -- **salicide**



Dielectric added, CMP applied, contact holes cut and metal 1 applied.



CMOS Process Enhancements

Multiple threshold voltages and oxide thicknesses:

Low threshold devices offer more I_{on} but have greater **subthreshold leakage** -- used on speed paths.

High V_t devices used elsewhere to minimize leakage.

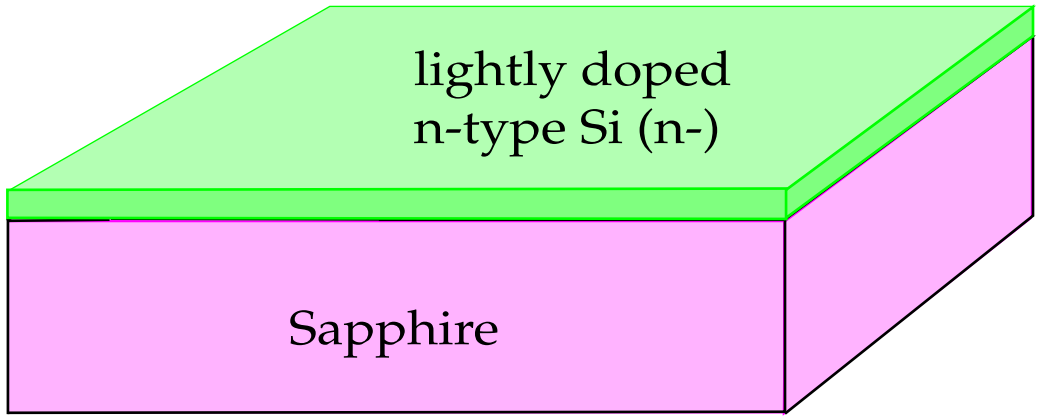
Thin gate oxides also enhance I_{on}, however, very thin oxides also add **gate leakage**.

Thicker gate oxides: I/O, *medium*: low leakage logic, *thin*: speed paths.

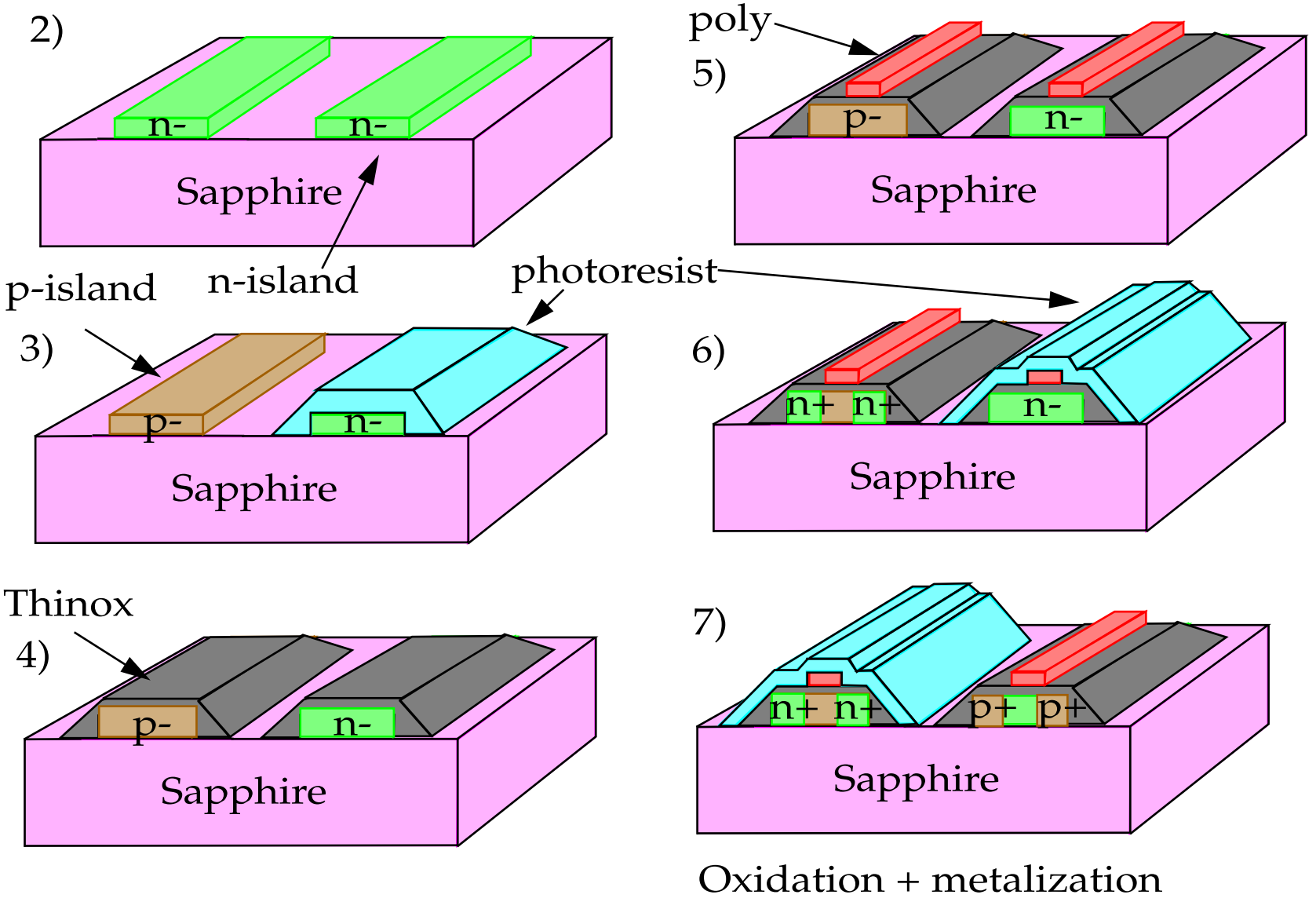
Silicon-On-Insulator (SOI) process:

Instead of silicon substrate, sapphire or SiO_2 is used.

1)



CMOS Processing Technology



CMOS Process Enhancements

High-k gate dielectrics:

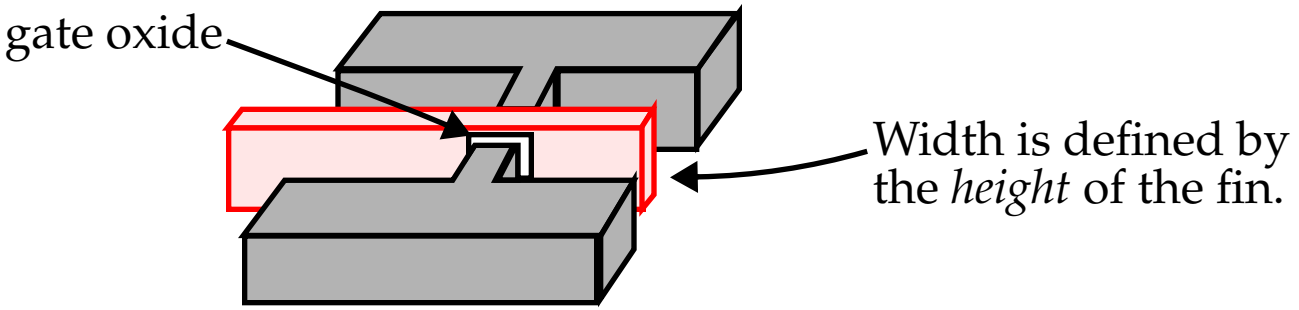
The need for large gate capacitance requires very thin oxides, but as indicated, gate leakage increases.

Proposed materials: *hafnium oxide*, HfO_2 (k=20), *zirconium oxide*, ZrO_2 (k=23) and *silicon nitride*, Si_3N_4 (k = 6.5-7.5) vs. SiO_2 with k=3.9.

Low-leakage transistors:

Subthreshold leakage (drain to source) caused by inability of gate to turn off the channel.

finfets represent a solution in which gate surrounds channel on three sides, instead of just on top.



CMOS Process Enhancements

Higher mobility transistors:

Silicon germanium (SiGe) has higher mobility (μ), improves I_{on} (and speed).

Popular for communication circuits because of good *radio frequency* (RF) performance (often better than III-V compounds such as GaAs and InP.

SiGe also used to improve speed in conventional MOS by creating *strained silicon*.

Implanted germanium atoms *stretch* the silicon lattice, improving mobility up to 70% (for a 30% performance increase).

Copper interconnect:

Copper has lower resistance than aluminum.

However, copper *diffuses* into silicon and dielectrics, destroying transistors.

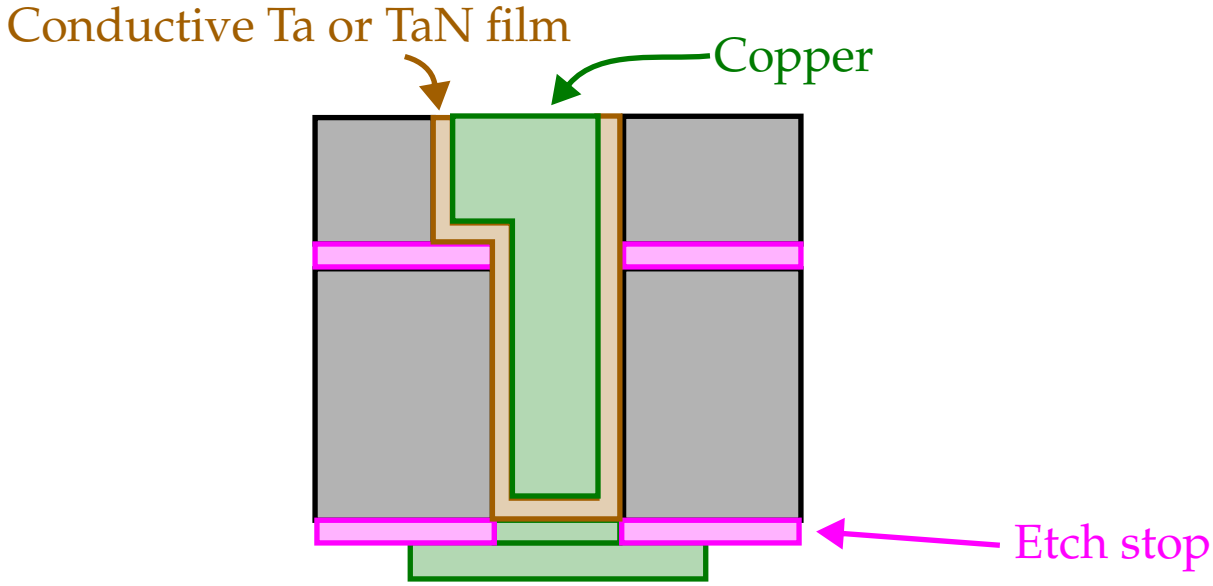
Also, etching is tricky and *copper oxide* increases contact Ω.

CMOS Process Enhancements

Copper interconnect:

To prevent contamination, *barrier layers* are created using a new metalization process called **damascene**.

Aluminum is subtractive (add everywhere and etch) while copper is additive, fill the trenches.



Low-k dielectrics:

Adding fluorine and carbon to SiO_2 reduces dielectric constant < 3.0

CMOS Process Enhancements

Mixed signal applications drive the need for high quality *resistors*, *capacitors*, *inductors* and *transmission lines*.

Many processes support special processing steps for these, e.g. *metal-insulator-metal* (MIM) capacitor.

In some cases, there is support for *non-volatile memory* (NVM).

Electrically erasable version today is called **flash** (we'll cover these at the end of the course).

When *npn* and *pnp* (bipolar) devices are available, the process becomes BiCMOS.

Other features include fuses, antifuses and MEMs devices.

Nanotechnology is a hot area -- seeks alternative structures to replace CMOS when scaling runs out of steam.

Carbon nanotude transistors are an example.

Layout or Design Rules

Design rules specify geometric constraints on the layout artwork.

Design rules represent the best compromise between *performance* and *yield*:

More conservative rules increase yield.

More aggressive rules increase performance.

Design rules represent a **tolerance** that ensures *high probability* of correct fabrication

They are NOT a *hard boundary* between correct and incorrect fabrication.

Two approaches to describing design rules

- λ-based rules: Allows first order scaling.

  To move a design from 4 μm to 2 μm, simply reduce the value of λ.

  Worked well for 4 μm processes down to 1.2 μm processes.

  However, in general, processes rarely shrink uniformly.

Layout or Design Rules

- Micron rules: List of minimum feature sizes and spacings for all masks.
  For example, 3.25 μm for contact-poly-contact (transistor pitch) and 2.75 μm metal 1 contact-to-contact pitch.

  Micron rules can result in as much as a 50% size reduction over λ rules.

  Normal style for industry.

The laboratory discussions will cover these in more detail.

Advanced technologies also have *antenna rules*, *layer density rules* and *resolution enhancement rules* (e.g. all poly is vertical OR horizontal, not both).