Basic Properties of a Digital Design

These help quantify the quality of a design from different perspectives:

- Cost
- Functionality
- Robustness
- Performance
- Energy consumption

Which of these criteria is important is dependent on the **application**:

Performance is important for compute servers.

Energy consumption is a dominant metric for cell-phones.

The following analysis focuses on the quality metrics of a simple inverter.

These carry forward to the analysis of more complex entities discussed later.

Before doing so, let's consider the **cost** of an integrated circuit.

Cost of an Integrated Circuit

Total cost of a product can be broken down into two basic components:

- *Recurring* expenses (**variable cost**).
- *Non-recurring* expenses (**fixed cost**).

Fixed cost is INdependent of sales volume.

Includes effort in time and manpower it takes to produce the design.

Indirect costs (company overhead that cannot be billed directly to one product), e.g., R&D, manufacturing equipment, marketing, etc.

Variable cost accounts for cost directly attributable to a manufactured product.

It is proportional to the product volume and includes:

- Material cost
- Assembly cost
- Testing cost

Total cost:

cost/IC = variable cost per IC + (fixed cost/volume)

Cost of an Integrated Circuit

It follows that:

- The impact of **fixed cost** is more pronounced for *small-volume* products.
- The design of a microprocessor can afford to support a large design team.

The cost to produce a transistor has dropped exponentially over the past decades.

However, the form of the equation for **variable cost** has not changed:

$$\text{Variable cost} = \frac{\text{Cost of die} + \text{Cost of die test} + \text{Cost of packaging}}{\text{Final test yield}}$$

$$\text{Cost of die} = \frac{\text{Cost of wafer}}{\text{Dies/wafer} \times \text{Die yield}}$$

We will focus on the *cost of the die* in this analysis.

It's clear that *Cost of die* is related to chip area.

The bigger the die, the more it costs since "Dies/wafer" gets smaller.

Cost of an Integrated Circuit

The actual relation between cost and area is more complex and depends on **die yield**.

Die yield is related to the number of defects, the size of the die and the complexity of the manufacturing process.

Under the assumptions that:

- Defects are randomly distributed over the wafer.
- Yield is inversely proportional to the complexity of the fabrication process.

Die yield can be expressed as:

$$\text{Die yield} = \left(1 + \frac{\text{Defects per unit area} \times \text{Die size}}{\alpha}\right)^{-\alpha}$$

α is related to the number of masks, a measure of process complexity.
It is approximately 3.0 today.

Defects per unit area depends heavily on the maturity of the process but the range 0.5 to 1.0 per cm^2 is typical.

Cost of an Integrated Circuit

For example, assume:

- Wafer size is 12 inches
- Die size is 2.5 cm^2
- 1 defects/cm^2
- α is 3

What is the die yield?

Dies per wafer (which takes into account the dies lost along the perimeter):

$$\text{Dies/wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

Plugging in yields 252 (=296 - 44) "potentially" operational die.

Plugging in for die yield gives **16%!**

Therefore, on average, only 40 dies will be functional.

Cost of an Integrated Circuit

The bottom line:

The number of good dies/wafer = dies/wafer * die yield.

The larger and/or more complex the chip, the more costly -- its NOT a **linear** relationship.

$$\text{Cost of die} = f(\text{die area})^4 \quad \text{for } \alpha = 3.0$$

The designer is going to be interested in using smaller gates, for two reasons:

- They reduce die size.
- Smaller gates tend to be **faster** and **consume less energy**.

  Total gate capacitance (a dominant performance parameter) often scales with area.

The # *of transistors* in a gate is often indicative of **implementation area**, although complex interconnect can cause *wiring area* to dominate.

Functionality and Robustness

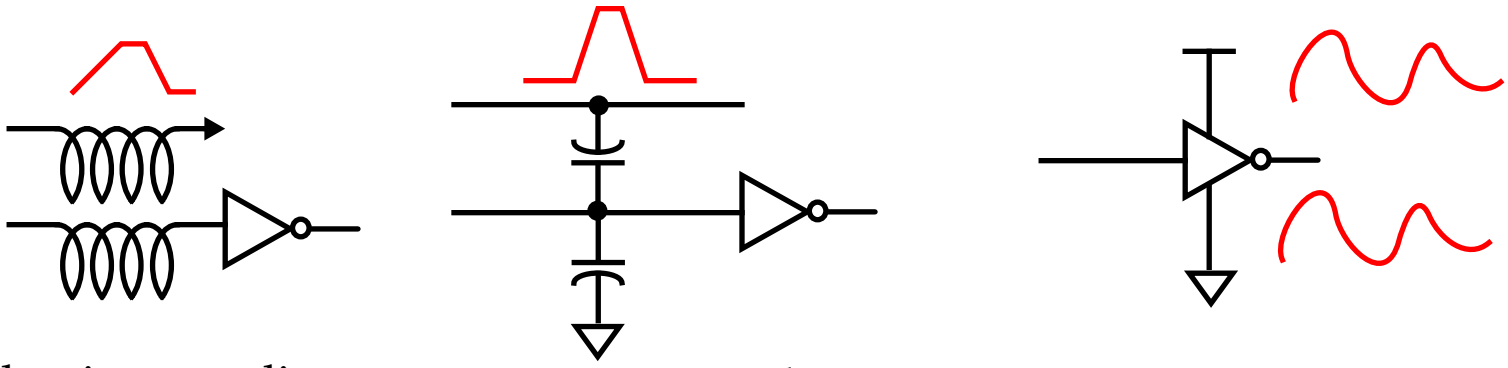
Measured behavior of a manufactured gate normally deviates from the expected response because:

- Variations in manufacturing process (**process variations**)

  Dimensions, *threshold voltage* and *currents* of a MOS transistor can vary significantly between runs, between wafers, and within chips.

- **Noise sources**

  Unwanted variations of voltages and currents at the logic nodes.



Inductive coupling Capacitive coupling Power and Ground Noise.

Most noise sources are **internal** and proportional to the logic swing while external noise source amplitudes are not related to signal levels.

Coping with these is a major challenge in high performance circuit design.

Functionality and Robustness

Steady-state parameters of a gate (static behavior) determine how robust it is to manufacturing and noise variations.

Their analysis requires an understanding of how digital signals are represented in electronic circuits.

The transformation of an *electrical voltage* into a *discrete* variable (logic value abstraction) is accomplished via the definition of nominal voltage levels.

- V_{OH}: High logic level.
- V_{OL}: Low logic level.

The difference between V_{OH} and V_{OL} is called the logic or signal swing, V_{sw}.

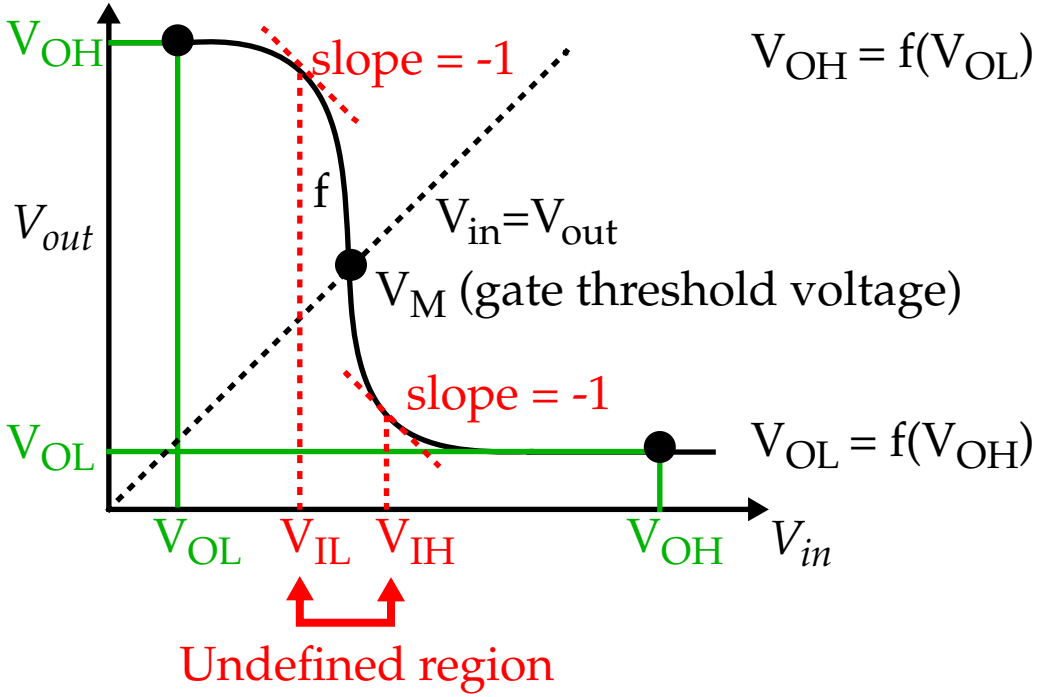
The electrical function of a gate is expressed by its *voltage-transfer characteristic* (**VTC**) or *DC transfer characteristic*.

Functionality and Robustness

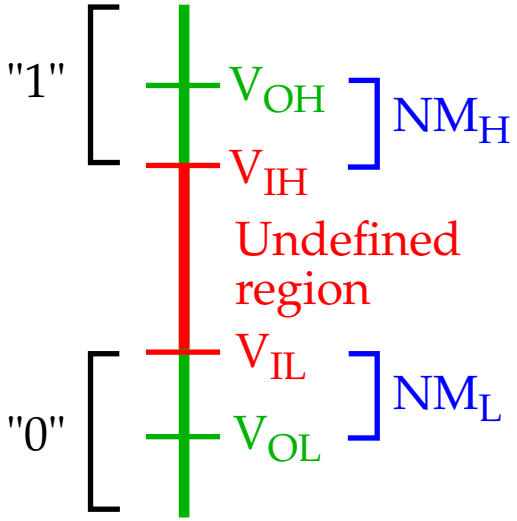
VTC for an inverter.

A graph that plots output voltage as a function of the input voltage:

$V_{out} = f(V_{in})$.



$V_{OH} = f(V_{OL})$



voltage -> logic

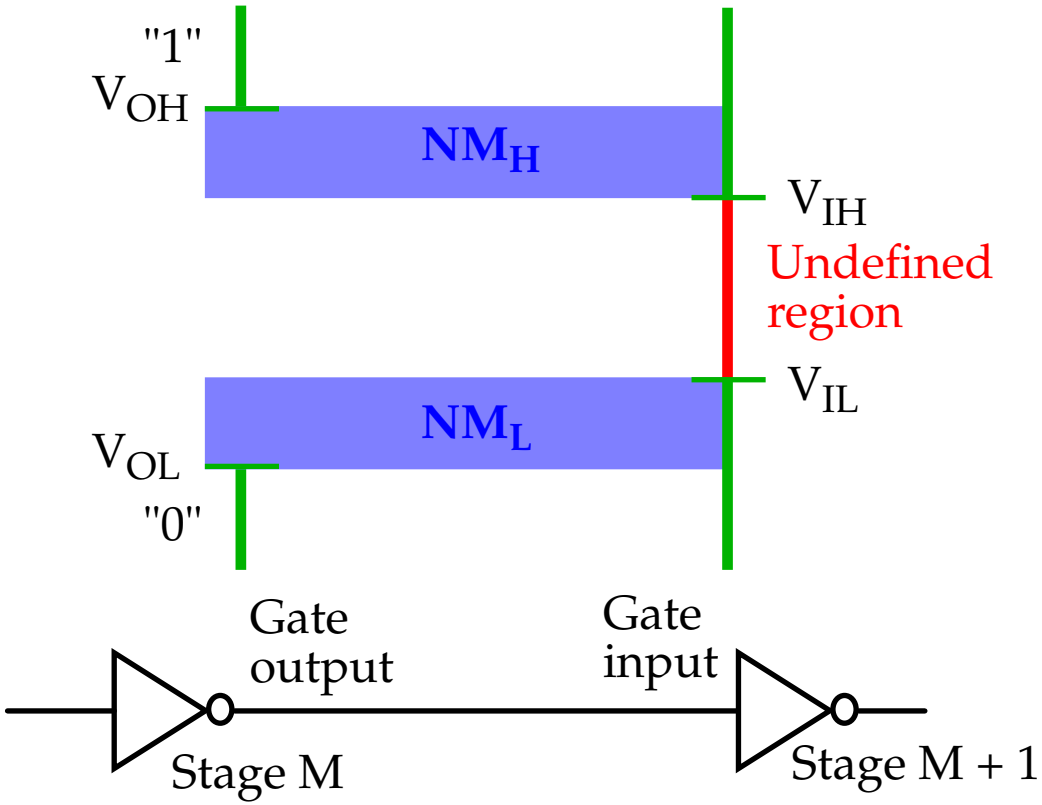
Even when an ideal input signal is applied to the input, the output often deviates from the ideal, due to noise and output loading.

Functionality and Robustness

Large "1" and "0" intervals are desirable.

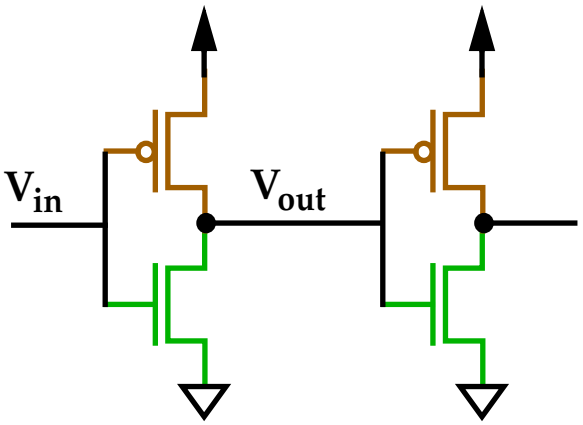
A measure of the sensitivity of a gate to noise is given by **noise margins**:

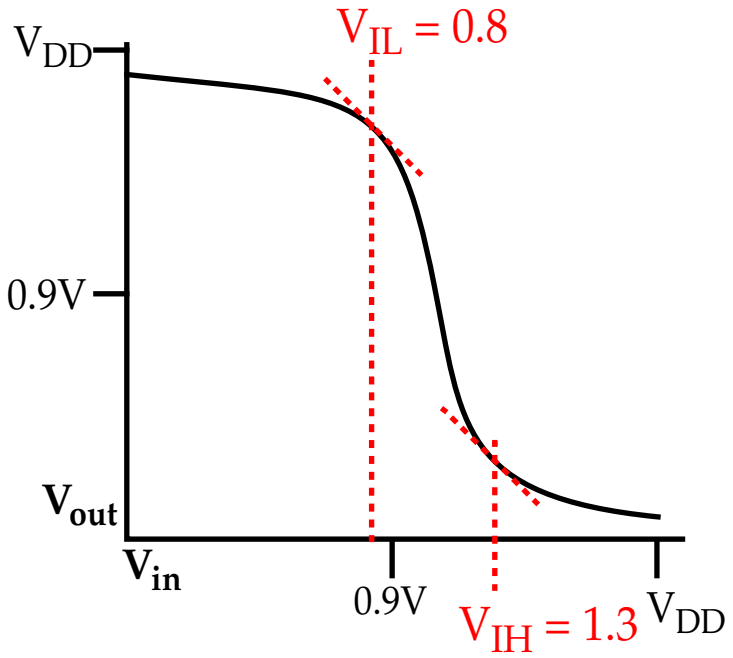
- NM_L (noise margin low) = V_{IL} - V_{OL}
- NM_H (noise margin high) = V_{OH} - V_{IH}



Functionality and Robustness

For example:





Assume output nominal voltages are:

- $V_{OH} = 1.7V$
- $V_{OL} = 0.1V$

$NM_L = V_{IL} - V_{OL} = 0.8 - 0.1 =$ **700mV**

$NM_H = V_{OH} - V_{IH} = 1.7 - 1.3 =$ **400mV**

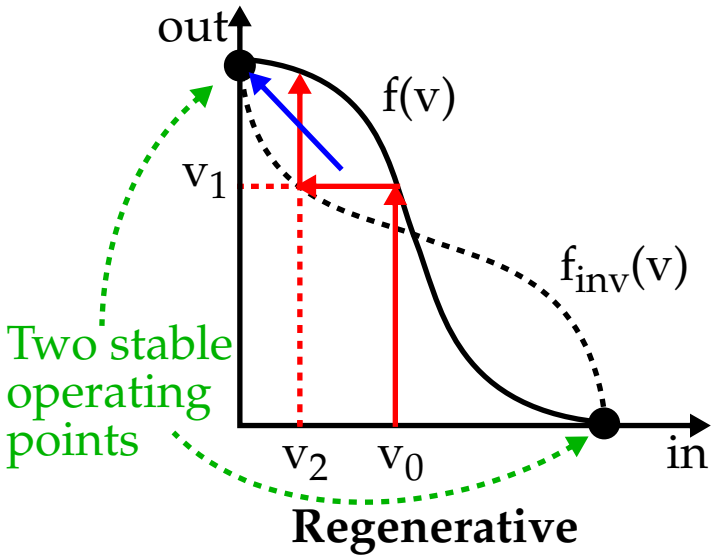
Functionality and Robustness

Regenerative Property:

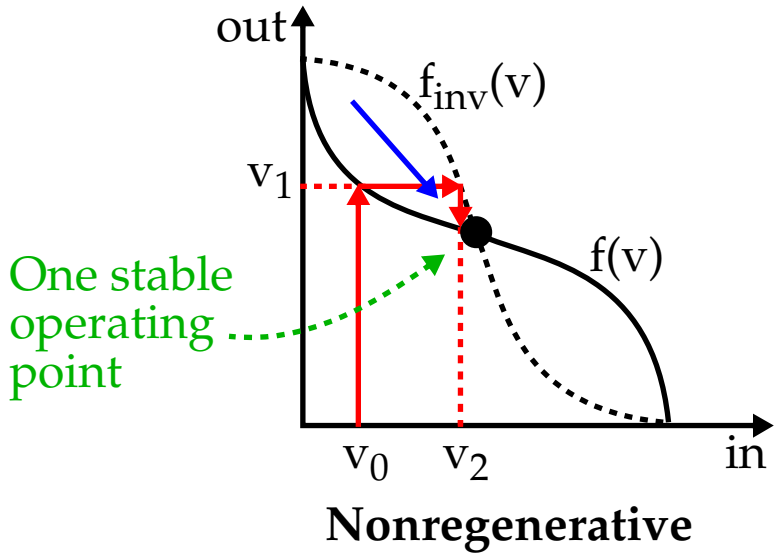
Large noise margins are desirable but **not** a sufficient requirement.

The gate must also possess the regenerative property.

It's regenerative if the *accumulation* of additional noise sources does NOT drive the signal into the undefined region.



Regenerative



Nonregenerative

Regenerative requires that the **|gain|** be *greater than 1* in the "transient" (undefined) region, bordered by regions with *gains less than 1*.

Points V_{IH} and V_{IL} define the borders.

Functionality and Robustness

Noise immunity

Noise margins expresses the capability of a circuit to "overpower" a noise source.

Noise immunity expresses the ability of a system to process and transmit information correctly in the *presence of noise*.

Many digital circuits with low noise margins have good noise immunity because the **reject a noise source** rather than overpower it.

These circuits allow only a small fraction of the noise source to couple to important circuit nodes.

Noise sources, as mentioned, are divided into:

- Sources proportional to the logic swing, V_{sw}:

  Impact on signal node is gV_{sw}.

- Sources that are fixed:

  Impact on signal node is fV_{Nf} with V_{Nf} is the **amplitude of noise source** and f is **transfer function** from noise source to signal node.

Functionality and Robustness

Noise immunity

Assume the noise margins are **half** the voltage swing.

For correct operation, the noise margins have to be *larger* than the sum of the noise values:

$$V_{NM} = \frac{V_{sw}}{2} \geq \sum_i f_i V_{Nfi} + \sum_j g_j V_{sw}$$

Therefore, the *minimum signal swing* necessary of system operation is:

$$V_{sw} \geq \frac{2\sum_i f_i V_{Nfi}}{1 - 2\sum_j g_j}$$

The signal swing (and noise margin) has to be large enough to overpower the fixed sources, $f_i V_{Nfi}$.

However, increasing V_{sw} does not work for internal sources.

Here, g_j must be small. (The impact of the internal sources is dependent upon the **noise suppressing capabilities** of the gate).