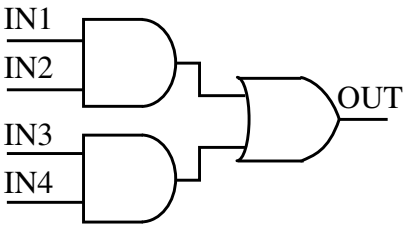
LAB Assignment #1 for ECE 595

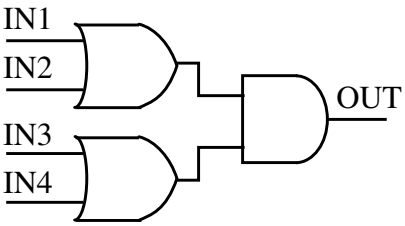
Assigned: Mon., Feb. 24, 2016
Due: Wed., Mar. 2, 2016

Description: Add 4-input AO and OA gates to the std cell library.

Design the schematic and layout for a 1X, 2X and 4X 4-input AO and OA following the rules and heuristics discussed in class regarding pin placement, routing grid, transistor sizing, cell height/ width, diffusion spacing from edge, using the design rules in the existing 90 nm standard cell library. Ensure that your inverter is DRC and LVS clean both by itself and when combined with other copies of itself (in any of the 4 orientations) in a test layout. You are allowed to discuss the problem with your colleagues but each of you must do your own layout.



4-input AO



4-input OA