Introduction

Genus is a Cadence tool designed to automate the process of behavioral to netlist synthesis

Slides drafted from
CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/LAB1

To run genus:

```
genus -f run.tcl
```

Cadence recommends running *write_template* to ensure attribute/variable settings are for latest release, and the tcl script uses the latest recommended synthesis flow

```
genus :> write_template -outfile <name>.tcl -full
```

The *-full* flag writes a template with all basic commands, DFT, power and retiming attributes

See documentation in <path_to_genus>/doc

Introduction

genus is a true tcl-based tool, using tcl language constructs including variables, lists, objects, attributes, directories and commands

For LAB1, the following will execute *genus*

```
genus -f run.tcl
```

A log file, *genus.logx*, will be generated, along with a file that stores the commands executed, *genus.cmdx*

The best way to learn what *genus* is doing is to open two xterm windows

- Run *genus* by itself in one window (no -f option)
- Edit the *run.tcl* file in the second window
- Cut-and-paste commands from the *run.tcl* file into the *genus* window

The following shows snapshots of the execution sequence for LAB1

The version I am running is *Version: 21.17-s066_1*

Genus LAB1 Execution

INPUT:

```
#### Template Script for RTL->Gate-Level Flow (generated from GENUS 17.10-p007_1)

if {[file exists /proc/cpuinfo]} {
  sh grep "model name" /proc/cpuinfo
  sh grep "cpu MHz"    /proc/cpuinfo
}

puts "Hostname : [info hostname]"
```

OUTPUT:

```
Cadence Genus(TM) Synthesis Solution.
Copyright 2023 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[16:14:46.082353] Configured Lic search path (21.01-s002):
 5280@ece46licsrv.ece.unm.edu

Version: 21.17-s066_1, built Wed Mar 15 06:43:30 PDT 2023
Options:
Date:    Thu Oct 31 16:14:46 2024
Host:    picard.ece.unm.edu (x86_64 w/Linux 3.10.0-1160.119.1.el7.x86_64)
 (8cores*32cpus*2physical cpus*Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz 11264KB)
 (131370808KB)
PID:     4466
```

Genus LAB1 Execution

OUTPUT (cont):

```
OS:      Red Hat Enterprise Linux Workstation release 7.9 (Maipo)

[16:14:46.417506] Periodic Lic check successful
[16:14:46.417528] Feature usage summary:
[16:14:46.417530] Genus_Synthesis
Checking out license: Genus_Synthesis

Loading tool scripts...
Finished loading tool scripts (12 seconds elapsed).

WARNING: This version of the tool is 596 days old.
@genus:root: 1> #### Template Script for RTL->Gate-Level Flow (generated from GENUS
 17.10-p007_1)
@genus:root: 2>
@genus:root: 2> if {[file exists /proc/cpuinfo]} {
  sh grep "model name" /proc/cpuinfo
  sh grep "cpu MHz"    /proc/cpuinfo
}
model name      : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
model name      : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
...
cpu MHz         : 1800.000
cpu MHz         : 1800.000
...
puts "Hostname : [info hostname]"
Hostname : picard.ece.unm.edu
```

Genus LAB1 Execution

INPUT:

```
##########################################################################
## Preset global variables and attributes
##########################################################################
set DESIGN dtmf_recvr_core
set GEN_EFF medium
set MAP_OPT_EFF high
set DATE [clock format [clock seconds] -format "%b%d-%T"]
set _OUTPUTS_PATH outputs_${DATE}
set _REPORTS_PATH reports_${DATE}
set _LOG_PATH logs_${DATE}
set_db / .init_lib_search_path  {. ../LIB}
set_db / .init_hdl_search_path  {. ../RTL}
set_db / .information_level 7
```

OUTPUT:

```
@genus:root: 4> set DESIGN dtmf_recvr_core
dtmf_recvr_core
@genus:root: 5> set GEN_EFF medium
medium
@genus:root: 6> set MAP_OPT_EFF high
high
@genus:root: 7> set DATE [clock format [clock seconds] -format "%b%d-%T"]
Oct31-16:21:34
@genus:root: 8> set _OUTPUTS_PATH outputs_${DATE}
outputs_Oct31-16:21:34
```

Genus LAB1 Execution

OUTPUT (cont):

```
@genus:root: 9> set _REPORTS_PATH reports_${DATE}
reports_Oct31-16:21:34
@genus:root: 10> set _LOG_PATH logs_${DATE}
logs_Oct31-16:21:34
@genus:root: 12> set_db / .init_lib_search_path  {. ../LIB}
  Setting attribute of root '/': 'init_lib_search_path' = . ../LIB
1 {. ../LIB}
@genus:root: 14> set_db / .init_hdl_search_path  {. ../RTL}
  Setting attribute of root '/': 'init_hdl_search_path' = . ../RTL
1 {. ../RTL}
@genus:root: 24> set_db / .information_level 7
  Setting attribute of root '/': 'information_level' = 7
1 7
```

INPUT:

```
@genus:root: 25> ################################################################
@genus:root: 26> ## Library setup
@genus:root: 27> ################################################################
@genus:root: 28>
@genus:root: 28>
@genus:root: 28> set_db / .library { ../LIB/slow.lib ../LIB/pll.lib  ../LIB/
 CDK_S128x16.lib  ../LIB/CDK_S256x16.lib  ../LIB/CDK_R512x16.lib}
```

Genus LAB1 Execution

OUTPUT:

These *Warning*s can be safely ignored

```
Threads Configured:8
Warning : Invalid value specified. [LBR-531]
        : Illegal value '0.9V' defined for attribute 'voltage_unit'. The attribute
 will be ignored. (File /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/
 Genus_CUI_RAK/LAB1/../LIB/slow.lib, Line 15)
        : Invalid value found for the attribute. Correct as per Liberty syntax.
Info    : Missing library level attribute. [LBR-516]
        : 'voltage_unit' unit not found in the library. Assuming '1 V'  (File /data2/
 VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/LAB1/../LIB/
 slow.lib, Line 8)
Info    : Missing library level attribute. [LBR-516]
       : slew_derate_from_library not specified in the library, using .lib default of
 1. (File /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/
 LAB1/../LIB/slow.lib, Line 8)
Info    : Missing a function attribute in the output pin definition. [LBR-518]
        : Functionality is missing at pin 'Y' for the cell 'HOLDX1'. (File /data2/
 VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/LAB1/../LIB/
 slow.lib, Line 32486)
...
```

Genus LAB1 Execution

OUTPUT:

These *Warning*s can be safely ignored

```
Message Summary for Library all 5 libraries:
 ********************************************
 Invalid value specified. [LBR-531]: 1
 Missing a function attribute in the output pin definition. [LBR-518]: 5
 Missing library level attribute. [LBR-516]: 2
 ********************************************
           Reading file '/data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/
Lab/Genus_CUI_RAK/LAB1/../LIB/slow.lib'
           Reading file '/data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/
Lab/Genus_CUI_RAK/LAB1/../LIB/pll.lib'
Warning : Libraries have inconsistent nominal operating conditions. In the Liberty
 library, there are attributes called nom_voltage, nom_process and nom_temperature.
 Genus reports the message, if the respective values of the 2 given .libs differ.
 [LBR-38]
        : The libraries are 'slow_1v0' and 'pll'.
       : This is a common source of delay calculation confusion and should be avoided.
...
Warning : Libcell has no area attribute.  Defaulting to 0 area. [LBR-43]
        : Assigning 0 area to library cell 'CDK_R512x16/CDK_R512x16'.
        : Specify a valid area value for the libcell.
Info    : An output library pin lacks a function attribute. [LBR-41]
        : Output pin 'CDK_R512x16/ROM_OUT[0]' has no function.
        : If the remainder of this library cell's semantic checks are successful, it
 will be considered as a timing-model (because one of its outputs does not have a
 valid function.
```

Genus LAB1 Execution

INPUT:

```
@genus:root: 29> ## PLE
@genus:root: 30> set_db / .lef_library  { ../LEF/gsclib045_tech.lef ../LEF/
 gsclib045_macro.lef ../LEF/pll.lef   ../LEF/CDK_S128x16.lef  ../LEF/CDK_S256x16.lef
 ../LEF/CDK_R512x16.lef   }
```

OUTPUT:

These *Warning*s can be safely ignored

```
 According to lef_library, there are total 11 routing layers [ V(5) / H(6) ]


Info    : Mismatch in unateness between 'timing_sense' attribute and the function.
 [LBR-155]
        : 'timing_sense' attribute between pin 'CI' and 'S' in libcell 'ADDFHX2' is
 'pos_unate', but unateness determined from function is 'non_unate'.
        : The 'timing_sense' attribute will be respected.
...
  Setting attribute of root '/': 'lef_library' = /data2/VLSI_SYNTHESIS_2024/
 CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/LAB1/../LEF/gsclib045_tech.lef /
 data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/LAB1/../
 LEF/gsclib045_macro.lef /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/
 Lab/Genus_CUI_RAK/LAB1/../LEF/pll.lef /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/con-
 tents/Module_3/Lab/Genus_CUI_RAK/LAB1/../LEF/CDK_S128x16.lef /data2/
 VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/LAB1/../LEF/
 CDK_S256x16.lef /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/
 Genus_CUI_RAK/LAB1/../LEF/CDK_R512x16.lef
...
```

Genus LAB1 Execution

INPUT:

```
@genus:root: 31> read_hdl " pllclk.v accum_stat.v alu_32.v arb.v data_bus_mach.v
 data_sample_mux.v decode_i.v decoder.v \
        digit_reg.v conv_subreg.v dma.v dtmf_recvr_core.v execute_i.v m16x16.v
 mult_32_dp.v \
        port_bus_mach.v prog_bus_mach.v ram_128x16_test.v ram_256x16_test.v
 results_conv.v spi.v \
        tdsp_core_glue.v tdsp_core_mach.v tdsp_core.v tdsp_data_mux.v tdsp_ds_cs.v
 test_control.v \
        ulaw_lin_conv.v power_manager.v "
```

OUTPUT:

```
            Reading Verilog file '../RTL/pllclk.v'
            Reading Verilog file '../RTL/accum_stat.v'
            Reading Verilog file '../RTL/tdsp.h'
assign #1 sign = accum[`S_ACC_SIGN] ;
          |
Warning : Ignoring unsynthesizable delay specifier (#<n>) mentioned in verilog file.
 These delay numbers are for simulation purpose only. [VLOGPT-35]
        : in file '../RTL/accum_stat.v' on line 68, column 9.
       : All delay numbers assigned or used in behavioral code are for simulation pur-
 poses only and are not synthesizable. These values are ignored during synthesis. This
 warning is issued only once per module.
            Reading Verilog file '../RTL/alu_32.v'
            Reading Verilog file '../RTL/tdsp.h'
            Reading Verilog file '../RTL/arb.v'
            Reading Verilog file '../RTL/data_bus_mach.v'
...
```

Genus LAB1 Execution

INPUT:

```
elaborate $DESIGN
```

OUTPUT:

Verilog warning, you should pay attention to these, as you do in Xilinx Vivado

```
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'dtmf_recvr_core' from file '../RTL/
 dtmf_recvr_core.v'.
Info    : Elaborating Subdesign. [ELAB-2]
        : Elaborating block 'power_manager' from file '../RTL/power_manager.v'.
Info    : Bitwidth mismatch in assignment. [CDFG-372]
        : Width of left hand side 'next_power_state' [3] doesn't match the width of
 right hand side [5] in assignment in file '../RTL/power_manager.v' on line 88.
...
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
Stage: post_elab
------------------------------------------------------------
| Trick              | Accepts | Rejects | Runtime (ms) |
------------------------------------------------------------
| ume_constant_bmux |       0 |       0 |         1.00 |
------------------------------------------------------------
...
```

Genus LAB1 Execution

INPUT:

```
puts "Runtime & Memory after 'read_hdl'"
time_info Elaboration
```

Prints timing information

INPUT:

```
check_design
```

OUTPUT:

More sanity checks on the design description

```
        Check Design Report (c)
         -------------------
 Summary
 -------

              Name                              Total
-------------------------------------------------
Unresolved References                             0
Empty Modules                                     0
Unloaded Port(s)                                  9
Unloaded Sequential Pin(s)                       17
Unloaded Combinational Pin(s)                   479
Assigns                                         197
...
```

Genus LAB1 Execution

INPUT:

```
check_design -unresolved
```

OUTPUT:

```
          Check Design Report (c)
          -----------------------


  Unresolved References & Empty Modules
  -------------------------------------
No unresolved references in design 'dtmf_recvr_core'
No empty modules in design 'dtmf_recvr_core'
  Done Checking the design.
```

INPUT:

```
read_sdc ../constraints/dtmf_recvr_core_gate.sdc
puts "The number of exceptions is [llength [vfind "design:$DESIGN" -exception *]]"
```

OUTPUT:

```
            Reading file '/data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/
 Lab/Genus_CUI_RAK/LAB1/../constraints/dtmf_recvr_core_gate.sdc'
Statistics for commands executed by read_sdc:
 "create_clock"              - successful      7 , failed      0 (runtime  0.01)
...
read_sdc completed in 00:00:00 (hh:mm:ss)
@genus:root: 38> puts "The number of exceptions is [llength [vfind "design:$DESIGN" -
 exception *]]"
The number of exceptions is 9
```

Genus LAB1 Execution

INPUT:

```
if {![file exists ${_LOG_PATH}]} {
  file mkdir ${_LOG_PATH}
  puts "Creating directory ${_LOG_PATH}"
}
if {![file exists ${_OUTPUTS_PATH}]} {
  file mkdir ${_OUTPUTS_PATH}
  puts "Creating directory ${_OUTPUTS_PATH}"
}
if {![file exists ${_REPORTS_PATH}]} {
  file mkdir ${_REPORTS_PATH}
  puts "Creating directory ${_REPORTS_PATH}"
}
```

OUTPUTS:

Makes directories for results

```
Creating directory logs_Oct31-16:21:34
...
```

INPUT:

```
set_db / .syn_generic_effort $GEN_EFF
```

OUTPUT:

```
 Setting attribute of root '/': 'syn_generic_effort' = medium
1 medium
```

Genus LAB1 Execution

INPUT:

```
syn_generic
```

OUTPUT:

Synthesis to generic gates: or2, nand2, complex2

```
      Running additional step before syn_gen...

Info    : Undriven module output port. [ELABUTL-128]
        : Assuming a logic '0' value for undriven bits of output port 't_sdo' in module
 'tdsp_core'.
        : The 'hdl_unconnected_value' attribute controls treatment of undriven output
 port.
...
Stage: pre_early_cg
...
Stage: pre_to_gen_setup/post_to_gen_setup
...
Stage: pre_hlo_rtlopt/pre_rtlopt/post_hlo_rtlopt/post_rtlopt
...
Stage: post_muxopt
...
Stage: to_generic
...
Stage : first_condense
...
```

Genus LAB1 Execution

INPUT:

```
puts "Runtime & Memory after 'syn_generic'"
time_info GENERIC
report_dp > $_REPORTS_PATH/generic/${DESIGN}_datapath.rpt
write_snapshot -outdir $_REPORTS_PATH -tag generic
report_summary -directory $_REPORTS_PATH
```

OUTPUT:

Reports runtime, timing analysis (slack), area estimate, power consumption estimate

```
Runtime & Memory after 'syn_generic'
@genus:root: 45> time_info GENERIC
stamp 'GENERIC' being created for table 'default'
...
================================================================================
Metric                              generic
================================================================================
Slack (ps):                          7,494
  R2R (ps):                          9,220
  I2R (ps):                          7,494
  R2O (ps):                         15,248
  I2O (ps):                       no_value
  CG  (ps):                       no_value
```

INPUT:

```
set_db / .syn_map_effort $MAP_OPT_EFF
```

Genus LAB1 Execution

INPUT:

```
syn_map
```

OUTPUT:

Maps generic gates to std cells available in library, new estimates on speed, power area

```
Info    : Ignoring specified timing sense. [LBR-170]
        : The 'timing_sense' definition 'positive_unate' for library pin 'TLATNSRX4/Q'
 is ignored.
...
                                      Capacitance
  Layer                                / Length          Data source:
Name         Direction Utilization  (pF/micron)        lef_library
-----------------------------------------------
M1               H         0.00        0.000412
M2               V         1.00        0.000416
...
Info    : Mapping. [SYNTH-4]
        : Mapping 'dtmf_recvr_core' using 'high' effort.
Mapper: Libraries have:
        domain _default_: 324 combo usable cells and 126 sequential usable cells
```

INPUT:

```
@genus:root: 51> puts "Runtime & Memory after 'syn_map'"
```

Output intermediate analysis results

Genus LAB1 Execution

INPUT:

```
write_do_lec -revised_design fv_map -logfile ${_LOG_PATH}/rtl2intermediate.lec.log >
 ${_OUTPUTS_PATH}/rtl2intermediate.lec.do
```

OUTPUT:

For verification of your design in *Conformal*, RTL to netlist verification tool

```
Info    : Wrote dofile. [CFM-1]
        : Dofile is 'outputs_Oct31-16:21:34/rtl2intermediate.lec.do'.
        : Alias mapping flow is enabled.
```

INPUT:

```
set_db / .syn_opt_effort $MAP_OPT_EFF
syn_opt
```

OUTPUT:

Optimization

```
@genus:root: 57> set_db / .syn_opt_effort $MAP_OPT_EFF
  Setting attribute of root '/': 'syn_opt_effort' = high
1 high
@genus:root: 58> syn_opt
Current PLE settings:

Aspect ratio        : 1.000
Shrink factor       : 1.000
...
```

Genus LAB1 Execution

INPUT:

```
write_snapshot -outdir $_REPORTS_PATH -tag final
```

OUTPUT:

Final metrics, slack, area, congestion, power, etc

```
%# Begin write_snapshot (10/31 17:49:01, mem=1708.38M)
%# Begin qos_stats (10/31 17:49:01, mem=1744.22M)
        Computing arrivals and requireds.
%# End qos_stats (10/31 17:49:01, total cpu=03:00:01, real=03:00:00, peak
 res=814.60M, current mem=1744.22M)


Working Directory = /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/
 Genus_CUI_RAK/LAB1
QoS Summary for dtmf_recvr_core
================================================================================
Metric                              generic         map             syn_opt
================================================================================
Slack (ps):                           7,494           1,658             844
  R2R (ps):                           9,220           1,658             844
  I2R (ps):                           7,494           7,274           7,274
  R2O (ps):                          15,248          15,148          15,148
  I2O (ps):                        no_value        no_value        no_value
  CG  (ps):                        no_value          15,678          15,678
...
```

Genus LAB1 Execution

INPUT:

```
write_sdc > ${_OUTPUTS_PATH}/${DESIGN}_m.sdc
```

OUTPUT:

```
Finished SDC export (command execution time mm:ss (real) = 00:01).
```

Genus LAB2 Execution -- DFT

INPUT: (SAME as LAB1)

```
@genus:root: 1> if {[file exists /proc/cpuinfo]} {
  sh grep "model name" /proc/cpuinfo
  sh grep "cpu MHz"    /proc/cpuinfo
}
puts "Hostname : [info hostname]"

@genus:root: 6> set DESIGN dtmf_recvr_core
dtmf_recvr_core
@genus:root: 7> set GEN_EFF medium
medium
@genus:root: 8> set MAP_OPT_EFF high
high
@genus:root: 9> set DATE [clock format [clock seconds] -format "%b%d-%T"]
Nov01-15:49:07
@genus:root: 10> set _OUTPUTS_PATH outputs_${DATE}
outputs_Nov01-15:49:07
@genus:root: 11> set _REPORTS_PATH reports_${DATE}
reports_Nov01-15:49:07
@genus:root: 12> set _LOG_PATH logs_${DATE}
logs_Nov01-15:49:07
@genus:root: 14> set_db / .init_lib_search_path {. ../LIB}
  Setting attribute of root '/': 'init_lib_search_path' = . ../LIB
1 {. ../LIB}
@genus:root: 16> set_db / .init_hdl_search_path {. ../RTL}
  Setting attribute of root '/': 'init_hdl_search_path' = . ../RTL
1 {. ../RTL}
```

Genus LAB2 Execution -- DFT

INPUT:

```
read_libs " ../LIB/slow.lib ../LIB/pll.lib  ../LIB/CDK_S128x16.lib  ../LIB/
 CDK_S256x16.lib  ../LIB/CDK_R512x16.lib "
read_physical -lef " ../LEF/gsclib045_tech.lef ../LEF/gsclib045_macro.lef ../LEF/
 pll.lef   ../LEF/CDK_S128x16.lef  ../LEF/CDK_S256x16.lef  ../LEF/CDK_R512x16.lef "
```

OUTPUT:

Alternative to *set_db*

```
Threads Configured:8
Warning : Invalid value specified. [LBR-531]
        : Illegal value '0.9V' defined for attribute 'voltage_unit'. The attribute
 will be ignored. (File /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/
 Genus_CUI_RAK/LAB2/../LIB/slow.lib, Line 15)
        : Invalid value found for the attribute. Correct as per Liberty syntax.
Info    : Missing library level attribute. [LBR-516]
        : 'voltage_unit' unit not found in the library. Assuming '1 V'  (File /data2/
 VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/LAB2/../LIB/
 slow.lib, Line 8)
Info    : Missing library level attribute. [LBR-516]
       : slew_derate_from_library not specified in the library, using .lib default of
 1. (File /data2/VLSI_SYNTHESIS_2024/CADENCE_EDU/contents/Module_3/Lab/Genus_CUI_RAK/
 LAB2/../LIB/slow.lib, Line 8)
Info    : Missing a function attribute in the output pin definition. [LBR-518]
...
```

Genus LAB2 Execution -- DFT

INPUT: (SAME as LAB1)

```
@genus:root: 26> read_hdl " pllclk.v accum_stat.v alu_32.v arb.v data_bus_mach.v
 data_sample_mux.v decode_i.v decoder.v \
        digit_reg.v conv_subreg.v dma.v dtmf_recvr_core.v execute_i.v m16x16.v
 mult_32_dp.v \
        port_bus_mach.v prog_bus_mach.v ram_128x16_test.v ram_256x16_test.v
 results_conv.v spi.v \
        tdsp_core_glue.v tdsp_core_mach.v tdsp_core.v tdsp_data_mux.v tdsp_ds_cs.v
 test_control.v \
        ulaw_lin_conv.v power_manager.v "

@genus:root: 27> elaborate $DESIGN

@genus:root: 28> puts "Runtime & Memory after 'read_hdl'"

@genus:root: 29> time_info Elaboration

check_design -unresolved

@genus:root: 31> read_sdc ../constraints/dtmf_recvr_core_gate.sdc

@genus:root: 32> puts "The number of exceptions is [llength [vfind "design:$DESIGN" -
 exception *]]"

...
```

Genus LAB2 Execution -- DFT

INPUT:

```
check_timing_intent
```

OUTPUT:

Sanity checks on clock, undriven pins reported

```
        Computing net loads.
        Tracing clock networks.
Info    : Multimode clock gating check is disabled. [TIM-1000]
        Levelizing the circuit.
        Computing delays.
        Computing arrivals and requireds.
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.17-s066_1
  Generated on:           Nov 01 2024  04:08:34 pm
  Module:                 dtmf_recvr_core
  Technology libraries:   slow_1v0
...

Lint summary
 Unconnected/logic driven clocks                              0
 Sequential data pins driven by a clock signal                3
 Sequential clock pins without clock waveform                 2
 Sequential clock pins with multiple clock waveforms          0
 Generated clocks without clock waveform                      0
 Generated clocks with incompatible options                   0
 Generated clocks with multi-master clock                     0
...
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 37>
 ################################################################################
@genus:root: 38> ## Define cost groups (clock-clock, clock-output, input-clock,
 input-output)
@genus:root: 39>
 ################################################################################
@genus:root: 40>
@genus:root: 40> ## Uncomment to remove already existing costgroups before creating
 new ones.
@genus:root: 41> ## delete_obj [vfind /designs/* -cost_group *]
@genus:root: 42>
@genus:root: 42> if {[llength [all_registers]] > 0} {
  define_cost_group -name I2C -design $DESIGN
  define_cost_group -name C2O -design $DESIGN
  define_cost_group -name C2C -design $DESIGN
  path_group -from [all_registers] -to [all_registers] -group C2C -name C2C
  path_group -from [all_registers] -to [all_outputs] -group C2O -name C2O
  path_group -from [all_inputs]  -to [all_registers] -group I2C -name I2C
}
@genus:root: 43> define_cost_group -name I2O -design $DESIGN
@genus:root: 44> path_group -from [all_inputs]  -to [all_outputs] -group I2O -name I2O
@genus:root: 45> foreach cg [vfind / -cost_group *] {
  report_timing -group [list $cg] >> $_REPORTS_PATH/${DESIGN}_pretim.rpt
}
```

Defines three classes of paths

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 49> set_db / .dft_scan_style muxed_scan
```

OUTPUT:

Set the scan style for all designs

```
  Setting attribute of root '/': 'dft_scan_style' = muxed_scan
1 muxed_scan
```

INPUT:

```
@genus:root: 50> set_db / .dft_prefix DFT_
```

OUTPUT:

Set the name used as a prefix for all scan related signals, including compression sigs

```
1 DFT_
```

INPUT:

```
@genus:root: 51> set_db / .dft_identify_top_level_test_clocks true
@genus:root: 52> set_db / .dft_identify_test_signals true
```

OUTPUT:

Automatically trace and identify test clocks and other signals, set, reset...

```
  Setting attribute of root '/': 'dft_identify_top_level_test_clocks' = true
1 true
...
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 53> set_db / .dft_identify_internal_test_clocks false
@genus:root: 54> set_db / .use_scan_seqs_for_non_dft false
```

OUTPUT:

More DFT control variables

```
  Setting attribute of root '/': 'use_scan_seqs_for_non_dft' = false
1 false
...
```

INPUT:

```
@genus:root: 55> set_db "design:$DESIGN" .dft_scan_map_mode tdrc_pass
```

OUTPUT:

Controls the mapping of FFs to their scan-equivalent FFs

```
  Setting attribute of design 'dtmf_recvr_core': 'dft_scan_map_mode' = tdrc_pass
1 tdrc_pass
```

INPUT:

```
@genus:root: 56> set_db "design:$DESIGN" .dft_connect_shift_enable_during_mapping 1
 tie_off
```

OUTPUT:

Controls connection of the shift_enable pin during mapping from FF to scan-FF

```
  Setting attribute of design 'dtmf_recvr_core': ...
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 57> set_db "design:$DESIGN" .dft_connect_scan_data_pins_during_mapping
 loopback
```

OUTPUT:

Similar but specifies how scan_data pins are handled

```
  Setting attribute of design 'dtmf_recvr_core':
 'dft_connect_scan_data_pins_during_mapping' = loopback
1 loopback
```

INPUT:

```
@genus:root: 58> set_db "design:$DESIGN" .dft_scan_output_preference auto
```

OUTPUT:

Specifies which scan FF output pin to use in the scan-data path

```
  Setting attribute of design 'dtmf_recvr_core': 'dft_scan_output_preference' = auto
1 auto
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 59> set_db "design:$DESIGN" .dft_lockup_element_type
 preferred_level_sensitive
@genus:root: 60> set_db "design:$DESIGN" .dft_mix_clock_edges_in_scan_chains true
```

OUTPUT:

For designs that use multiple clocks/edges of the test clock in the same scan path

```
  Setting attribute of design 'dtmf_recvr_core': 'dft_lockup_element_type' =
 preferred_level_sensitive
1 preferred_level_sensitive
```

INPUT:

```
@genus:root: 61> define_test_clock -name scanclk -period 18000 scan_clk
```

OUTPUT:

Specifies the test clock and test-clock waveform, which is typically different than system clock

```
Info    : Added DFT object. [DFT-100]
        : Added test clock domain 'scanclk'.
Info    : Added DFT object. [DFT-100]
        : Added test clock 'scanclk'.
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 62> define_shift_enable -name se -active high scan_en
```

OUTPUT:

Specify the name and active value of the input signal that enables scan

```
Info    : Added DFT object. [DFT-100]
        : Added shift enable signal 'se'.
test_signal:dtmf_recvr_core/se
```

INPUT:

```
@genus:root: 63> define_test_mode -name tm -active high test_mode
```

OUTPUT:

Specifies the input signal name and constant value to use when in test mode

```
Info    : Added DFT object. [DFT-100]
        : Added test mode signal 'tm'.
test_signal:dtmf_recvr_core/tm
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 64> define_scan_chain -name top_chain -sdi scan_in -sdo scan_out -
 shift_enable se -create_ports
```

OUTPUT:

Create the scan chain or analyze an existing scan chain with the specified input and output

```
Info    : Added DFT object. [DFT-100]
        : Added scan chain 'top_chain'.
Info    : Created DFT port. [DFT-130]
        : Created scan data input port 'scan_in' in module 'dtmf_recvr_core'.
        : A port for DFT purposes was created.
Info    : Created DFT port. [DFT-130]
        : Created scan data output port 'scan_out' in module 'dtmf_recvr_core'.
Info    : Added scan chain. [DFT-151]
        : scan chain successfully defined.
scan_chain:dtmf_recvr_core/top_chain
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 65> check_dft_rules > $_REPORTS_PATH/${DESIGN}-tdrcs
```

OUTPUT:

Sanity checks on the scan chain just created

```
  Checking DFT rules for 'dtmf_recvr_core' module under 'muxed_scan' style

Info    : Auto detection of Async control signal. By default, all Async set and reset
 control signals of flops are identified automatically and an automatically generated
 test signal is added to the DFT setup, if no test signal is defined for them, yet.
 [DFT-303]
        : Setting PI async signal 'reset' to level '0' in test mode

...
Info    : Added DFT object. [DFT-100]
        : Added test mode signal 'reset'.
...         : Setting PI async signal 'spi_fs' to level '0' in test mode

Info    : Added DFT object. [DFT-100]
        : Added test mode signal 'spi_fs'.
Detected 0 DFT rule violation(s)
    ... see the log file for more details
  Number of user specified non-Scan registers:   0
      Number of registers that fail DFT rules:   0
      Number of registers that pass DFT rules: 550
  Percentage of total registers that are scannable: 100%
0
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 66> report_scan_registers > $_REPORTS_PATH/${DESIGN}-DFTregs
@genus:root: 67> report_scan_setup > $_REPORTS_PATH/${DESIGN}-DFTsetup_tdrc
```

OUTPUT:

Report generation, more details on the auto generated scan chain

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 68> set_db / .syn_generic_effort $GEN_EFF
```

OUTPUT:

Same process now without DFT

```
  Setting attribute of root '/': 'syn_generic_effort' = medium
1 medium
```

INPUT:

```
@genus:root: 69> syn_generic
```

OUTPUT:

Scan has little to do with synthesis to generic gates (search scan in genus.log)

```
##>Main Thread Summary:
##>-------------------------------------------------------------------------------
 ------
##>STEP                              Elapsed       WNS       TNS      Insts      Area
 Memory
##>-------------------------------------------------------------------------------
 ------
##>G:Initial                           0         -         -     13910    263739       400
##>G:Setup                             0         -         -         -         -         -
...
```

Genus LAB2 Execution -- DFT

There are LOTs of options at this point in the flow that relate to

- Shadow logic
- JTAG
- MBIST
- Boundry scan
- etc

INPUT:

```
@genus:root: 70> set_db / .syn_map_effort $MAP_OPT_EFF
```

OUTPUT:

Mapping

```
  Setting attribute of root '/': 'syn_map_effort' = high
1 high
```

INPUT:

```
@genus:root: 71> syn_map
```

OUTPUT:

Same process flow

...

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 72> puts "Runtime & Memory after 'syn_map'"
@genus:root: 73> time_info MAPPED
@genus:root: 74> write_snapshot -outdir $_REPORTS_PATH -tag map
@genus:root: 75> report_summary -directory $_REPORTS_PATH
@genus:root: 76> report_dp > $_REPORTS_PATH/map/${DESIGN}_datapath.rpt
```

OUTPUT:

Report generation, details about the map operation

```
...
QoS Summary for dtmf_recvr_core
================================================================================
Metric                              map
================================================================================
Slack (ps):                       1,302
  R2R (ps):                       1,302
  I2R (ps):                       7,190
  R2O (ps):                      14,928
  I2O (ps):                    no_value
  CG  (ps):                      15,604
TNS (ps):                            0
  R2R (ps):                          0
  I2R (ps):                          0
  R2O (ps):                          0
  I2O (ps):                    no_value
  CG  (ps):                          0
...
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 76> report_dp > $_REPORTS_PATH/map/${DESIGN}_datapath.rpt
@genus:root: 77> foreach cg [vfind / -cost_group *] {
  report_timing -group [list $cg] > $_REPORTS_PATH/${DESIGN}_[vbasename
 $cg]_post_map.rpt
}
@genus:root: 78> write_do_lec -revised_design fv_map -logfile ${_LOG_PATH}/
 rtl2intermediate.lec.log > ${_OUTPUTS_PATH}/rtl2intermediate.lec.do
```

OUTPUT:

More reporting, and then writing of *lec* do file, for *Conformal*, RTL to netlist verification tool

INPUT:

```
@genus:root: 79> set_db / .syn_opt_effort $MAP_OPT_EFF
  Setting attribute of root '/': 'syn_opt_effort' = high
1 high
@genus:root: 80> syn_opt
```

OUTPUT:

Last of synthesis steps, same as without DFT

```
Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'dtmf_recvr_core'.
        Computing net loads.
...
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 81> write_snapshot -outdir $_REPORTS_PATH -tag syn_opt
@genus:root: 82> report_summary -directory $_REPORTS_PATH
@genus:root: 83> puts "Runtime & Memory after 'syn_opt'"
@genus:root: 84> time_info OPT
@genus:root: 85> foreach cg [vfind / -cost_group *] {
  report_timing -group [list $cg] > $_REPORTS_PATH/${DESIGN}_[vbasename
 $cg]_post_opt.rpt
}
```

OUTPUT:

Reporting

INPUT:

```
@genus:root: 86> check_dft_rules -advanced
```

OUTPUT:

Re-run DFT rule checker, look for violations

```
Detected 0 DFT rule violation(s)
        Summary of check_dft_rules
        **************************
        Number of usable scan cells: 48
Clock Rule Violations:
----------------------
          Internally driven clock net: 0
...
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 87> connect_scan_chains -auto_create_chains
```

OUTPUT:

Build the scan chains

```
    Processing techlib slow_1v0 for muxed_scan scan cells
      Identified a usable, flop scan cell 'SDFFHQX8'
         active clock edge:  rising
      Identified a usable, flop scan cell 'SDFFNSRX2'
         active clock edge: falling
      Identified a usable, flop scan cell 'SDFFNSRXL'
         active clock edge: falling
      Identified a usable, flop scan cell 'SDFFQX1'
         active clock edge:  rising
      Identified a usable, flop scan cell 'SDFFRHQX1'
         active clock edge:  rising
      Identified a usable, flop scan cell 'SDFFRHQX4'
         active clock edge:  rising
      Identified a usable, flop scan cell 'SDFFRX1'
         active clock edge:  rising
      Identified a usable, flop scan cell 'SDFFRX2'
         active clock edge:  rising
...
Mapping DFT logic introduced by scan chain connection...
Mapping DFT logic done.
1
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 88> report_scan_chains > $_REPORTS_PATH/${DESIGN}-DFTchains
```

OUTPUT:

Scan chain report

```
Reporting 1 scan chain (muxed_scan)

Chain 1: top_chain
  scan_in:      scan_in_1
  scan_out:     scan_out_2
  shift_enable: scan_en (active high)
  clock_domain: scanclk (edge: mixed)
  length: 517
    bit 1       RESULTS_CONV_INST_go_reg  <scan_clk (fall)>
    bit 2       RESULTS_CONV_INST_lower770_dout_reg[0]  <scan_clk (fall)>
    bit 3       RESULTS_CONV_INST_lower770_dout_reg[1]  <scan_clk (fall)>
    bit 4       RESULTS_CONV_INST_lower770_dout_reg[2]  <scan_clk (fall)>
    bit 5       RESULTS_CONV_INST_lower770_dout_reg[3]  <scan_clk (fall)>
    bit 6       RESULTS_CONV_INST_lower770_dout_reg[4]  <scan_clk (fall)>
    bit 7       RESULTS_CONV_INST_lower770_dout_reg[5]  <scan_clk (fall)>
...
    bit 515     TDSP_CORE_INST_TDSP_CORE_MACH_INST_tdsp_state_reg[2]  <scan_clk
 (rise)>
    bit 516     TDSP_DS_CS_INST_t_bit_7_reg  <scan_clk (rise)>
    bit 517     TDSP_DS_CS_INST_t_sel_7_reg  <scan_clk (rise)>
------------------------
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 89> set_db / .syn_opt_effort low
@genus:root: 90> syn_opt -incremental
@genus:root: 91> write_snapshot -outdir $_REPORTS_PATH -tag syn_opt_low_incr
@genus:root: 92> report_summary -directory $_REPORTS_PATH
@genus:root: 93> puts "Runtime & Memory after 'syn_opt'"
@genus:root: 94> time_info INCREMENTAL_POST_SCAN_CHAINS
```

OUTPUT:

If timing is not met, re-run incremental optimization

```
...
```

INPUT:

```
@genus:root: 95> report_scan_setup > $_REPORTS_PATH/${DESIGN}-DFTsetup_final
```

OUTPUT:

Final report on scan chain insertion

```
Design Name
===========
    dtmf_recvr_core

Scan Style
==========
    muxed_scan
Design has a valid DFT rule check status
...
```

Genus LAB2 Execution -- DFT

INPUT:

```
@genus:root: 97> write_scandef > ${DESIGN}-scanDEF
@genus:root: 98> write_dft_abstract_model > ${DESIGN}-scanAbstract
scan style is muxed_scan
@genus:root: 99> write_hdl -abstract > ${DESIGN}-logicAbstract
@genus:root: 100> write_script -analyze_all_scan_chains > ${DESIGN}-writeScript-ana-
 lyzeAllScanChains
Warning : This command will be obsolete in a next major release. [TUI-37]
        : Use 'write_db -common' for saving design databases to operate with other
 Cadence tools. Use 'write_design' in future releases for saving files for operations
 with non-Cadence tools.
```

OUTPUT:

scanDEF file, verilog black-box header module, etc

```
VERSION 5.5 ;
NAMESCASESENSITIVE ON ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;
DESIGN dtmf_recvr_core ;
SCANCHAINS 2 ;
  - top_chain_seg1_scanclk_falling
    + PARTITION p_scanclk_falling
      MAXBITS 129
    + START PIN scan_in_1
    + FLOATING
       RESULTS_CONV_INST_go_reg ( IN SI ) ( OUT QN )
...
```

Genus LAB2 Execution -- DFT

INPUT:

```
report_dp > $_REPORTS_PATH/${DESIGN}_datapath_incr.rpt
report_messages > $_REPORTS_PATH/${DESIGN}_messages.rpt
write_snapshot -outdir $_REPORTS_PATH -tag final
report_summary -directory $_REPORTS_PATH
write_sdc > ${_OUTPUTS_PATH}/${DESIGN}_m.sdc
write_do_lec -golden_design fv_map -revised_design ${_OUTPUTS_PATH}/${DESIGN}_m.v -
 logfile  ${_LOG_PATH}/intermediate2final.lec.log > ${_OUTPUTS_PATH}/
 intermediate2final.lec.do
puts "Final Runtime & Memory."
time_info FINAL
puts "============================"
puts "Synthesis Finished ........."
puts "============================"

file copy [get_db / .stdout_log] ${_LOG_PATH}/.
```

OUTPUT:

Wrap up

...