

# ECE595: Advanced VLSI Design

**Course:**

ECE 595: Advanced VLSI Design, 3 credits.

**Course Instructor:**

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**Text:**

Neil H.E. Weste, David Harris, "CMOS VLSI Design", 4th edition, Addison Wesley, ISBN 10: 0-321-54774-8, ISBN 13: 978-0-321-54774-3

**Supplementary text:**

Erik Brunvand, "Digital VLSI Chip Design with Cadence and Synopsys CAD Tools", ISBN 0-13-509470-4

**Grading:**

The distribution of weights for the exams, homeworks and projects is as follows:

Exam	30%
Labs/Homework	30%
Project	30%
Class Participation	10%

No incompletes will be given, except as required by university policy for truly exceptional circumstances.

The final exam is cumulative. However, material covered after the second exam will be emphasized.

Students are encouraged to participate in class.

**Cheating at any time in this course will cause you to fail the course.**

**For a complete description of academic dishonesty, refer to the UNM Student Handbook.**

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## Course Outline:

Date	Lecture	Lab Assignment
Week 1	Introduction	CADENCE setup
Week 2	Design Methodologies	CADENCE virtuoso/composer
Week 3	Design Flows	CADENCE std cell library
Week 4	Design Economics	CADENCE std cell library
Week 5	Data Sheets and Doc	Behavioral to structural synthesis
Week 6	ASIC and Custom design	Abstract Generator
Week 7	CMOS Physical Design Styles	Place and Route
Week 8	mid-term exam	Place and Route
Week 9	Interchange Formats	Clock tree insertion
Week 10	Advanced Topics in Synthesis	Scan chain and I/O pad insertion
Week 11	Advanced Topics in Synthesis	Power/delay optimization
Week 12	Advanced Topics in Physical Synthesis	Hard macro insertion/GDS II
Week 13	Advanced Topics in Physical Synthesis	Chip Project
Week 14	Thanksgiving	Chip Project
Week 15	Advanced Topics in Power/Delay optimization	Chip Project
Week 16	Advanced Topics in Testability, Reliability, DFM, etc.	Chip Project
	Final exam	

(Note: Changes/Additions to this schedule will be posted on my web site <http://www.ece.unm.edu/~jimp>)