Cadence Encounter Library Characterizer – Tutorial

Abstract

This tutorial explains characterizing the Standard Cells using Cadence Encounter Library Characterizer (ELC) tool. It explains the flow of ELC tool which converts extracted version of standard cells to Liberty (.lib) or Cadence Encounter place and route tool's input file format (.tlf).

Steps for Running Encounter Library Characterizer

Step 1: Create Extracted Netlist

To characterize standard cells we need the extracted views of the standard cells. Let us create a subdirectory for the ELC under cadence working directory. Now create a schematic which contains an instance of all of your cells without connecting them. Then start ADE tool from there. Since we want extracted netlist with parasitics specify the extracted view in Setup \rightarrow Environment as shown in the screenshot below. (It can be extracted/analog_extracted/caliber depends on your simulator)



Environment Options			
Switch View List	calibre spectre cmos_sch cmos.sch schematic veriloga		
Stop View List	spectre		
Parameter Range Checking File			
Analysis Order			
Print Comments			
userCmdLineOption			
Automatic output log	⊻		
Use SPICE Netlist Reader(spp):			
savestate(ss):	V N		
recover(rec):			
	OK Cancel Defaults Apply Help		

Then generate the extracted netlist from Simulation \rightarrow Netlist \rightarrow Create as shown in the screenshot. Save this netlist file to your working directory with some preferred name (Eg: std_cells.scs).

Session Setup Analyses Variables Netlist and Run Run Stop Netlist and Run Run Stop Name Value Type Device Checking Outputs Juments Acconcerter Display Convergence Aids Acconcerter Display Recreate Outputs Name/Signal/Expr Value Value<	👫 🛛 Virtuoso® Analog Design	Environment (2) - Mosis_Chip_Std_Cells INV calibre 🛛 🗕	
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Plotting mode: Replace	III Status: Ready T=27 C Simulator: sp Design Variables	Netlist and Run Run Analyses Stop Device Checking Options Netlist Output Log Convergence Aids Recreate Outputs Name/Signal/Expr Value Plotting mode:	AC DC Trans

Step 2: Create ELC Configuration file

The configuration file has a set of commands that does some configurations for the ELC. Some of the examples are:

set_var SG_SPICE_SIMPLIFY true - This setting will put SignalStorm into "SIMPLE" mode for the purposes of inferring logic in your transistor structures.

set_var SG_HALF_WIDTH_HOLD_FLAG true - This setting is required for accurate analysis of your sequential circuits (such as flip-flops).

set_var SG_SIM_USE_LSF 1
set_var SG_SIM_LSF_CMD ""
set_var SG_SIM_LSF_PARALLEL 10

These settings will setup SignalStorm to run its simulation processes on the local machine using LSF (Load Sharing Facility) as opposed to using the distibuted server-farm (cluster) approach.

```
set_var SG_SIM_TYPE "spectre"
set var SG_SIM_NAME "spectre"
```

These settings will setup spectre as the simulation environment as opposed to HSPICE which is used by default. If you're wondering why the default simulator in a Cadence produce is HSPICE (a Synopsys product) rather than Spectre (a Cadence product). Please refer the attached sample configuration file.

We will also specify the characterization inputs like subcircuit name, model file (this comes with the PDK) and the setup file (which is explained in the next section)

Step 3: Create ELC Setup file

The setup file defines some setup required for the simulation. It defines the following:

- 🛛 🗮 Defines the Voltage, Temperature & Vth for typical, best and worst case
- * Defines also Resistance, transient time to simulate etc...

Save it with the file name under the ELC subdirectory with the name setup.ss. Please refer the attached setup file.

Step 4: Create Command file

You can start ELC by typing "elc" and then run it by typing a series of commands to run the simulation or can put those commands in a file called command file and run with a single command. I prefer creating a command file and running with a single command. This file essentially will have the following commands:

```
db_open std_cells \rightarrow Opens the working library
```

db_prepare –f \rightarrow

```
db_spice -s spectre -keep_log → This command will launch the simulation processes
db_output -lib std_cells.lib - process typical - state → saves output in Liberty file format
db_close
```

exit

Step 5: Run ELC

Now we can run the ELC with the following command and its parameters:

elc -L test.log -C test cmd.log -S cmd file

- Runs the ELC tool with the commands in cmd_file,
- test.log will have execution log
- test_cmd.log will have command log

Step 6: Convert Liberty file to Cadence Timing file

Now we can convert the Liberty file to Cadence timing file (.tlf) which will be used by Encounter tool.

```
syn2tlf std_cells.lib -format 4.3 -ir 50 -if 50 -dr 50 -df 50 -sr 10 -sf 10
-tr 90 -tf 90 -slew_measure_lower_rise 20 -slew_measure_lower_fall 20 -
slew_measure_upper_rise 80 -slew_measure_upper_fall 80 -o std_cells.tlf
```

This converts the Liberty file which is the output of the previous step to TLF file which is the cell library specification for Encounter Place & Route tool. Timing Library Format (.tlf) file will have the Timing and power parameters associated with the standard cells. Raise and Fall time delay & Power parameters in table format. Also has some I/O pin details

If you open and read the .tlf file, you can understand the rise & fall time and power analysis values. Unfortunately ELC doesn't give layout area information????