National Science Foundation Workshop on Future Research Directions in Testing of Electronic Circuits and Systems

May 12-13, 1998
Santa Barbara, CA
Workshop Report

1. Introduction

The goals of the meeting were (1) to identify emerging and mature research areas within the VLSI testing field in order to help focus the field on research necessary to develop algorithms and techniques for testing VLSI circuits and systems designed using future technologies, (2) to address issues related to increasing the impact of the VLSI test field on education in electrical and computer engineering, and (3) to identify models and mechanisms for enhancing the interaction, collaboration and data-sharing between industry and academia.

To facilitate focused discussion at the meeting, an electronic survey was conducted prior to the meeting. A list of 8 survey questions regarding test research topics, education, and interaction between academia and industry was sent to about 50 test researchers. More than 40 responses were received. A summary of the survey responses is given in Section 3. The complete responses and the participants of the survey are included in the appendix.

A two-day meeting was held in Santa Barbara, California on May 12 and 13, 1998. There was a total of 21 participants - 9 from academia, 11 from industry and one from NSF. Each participant presented a position statement at the meeting. The meeting then broke up into four working groups:

• Group A: Emerging and mature research topics related to high levels of abstraction,
• Group B: Emerging and mature research topics related to low levels of abstraction,
• Group C: Industry and university interaction/collaboration, and
• Group D: Education.

Issues and research topics raised in the survey responses and the position statements were thoroughly discussed in the working group meetings. This summary report contains findings and recommendations from these four working groups. These represent the collective views of the people participating in the workshop meeting with guidance taken from the electronic survey responses.

2. Findings and Recommendations

2.1 Emerging and Mature Research Topics

The SIA roadmap contains a variety of projections for chip characteristics and includes a section on test. Several of these projections have major impact on test research; for example, chip gate count is projected to increase by 30% per year while the pin count increases at a lower rate. On-chip clock speed increases dramatically while the tester Overall Timing Accuracy (OTA) does not. This trend implies increasing yield loss (estimated to be up to 48% by 2012) as guardbanding to cover tester errors results in the loss of more and more good chips. The volume of test data per gate is expected to remain constant, which implies that much more data needs to get across the chip boundary, resulting in bandwidth problems. Background IDDQ increases inexorably and the spread of IDDQ distribution is also increasing. IDDQ testing must be adapted to exist
in an environment of decreasing signal to noise ratio, or be replaced with a better suited method that maintains its effectiveness in defect screening and reliability prediction. Analog and mixed signal circuitry will be included on most high-end chips and thus cost-effective methods to test it will be needed. Also, conventional issues of overhead will be replaced by new problems. For example, wires will cost more than gates, both in silicon area and delay. Because Moore’s law shows no sign of abating, it is vital that any solutions developed are able to scale as design size increases.

Research which includes development of tools or methodologies as a byproduct must be aware of tool flows. Test tools need to fit into an overall design flow which includes synthesis, floorplanning, place and route, timing and power analysis. A "generic" tool flow is available in the SIA roadmap. Circuit design is moving toward a core-based, high reuse methodology. Test tools must be aware of this and fit into this flow. Flows especially need to be considered when a tool makes a modification to the design.

There is a strong need to base test theory on experimental data. We are aware of the difficulties of collecting useful test data, but also believe that this is the only way to validate the test theories and techniques.

In the following, we include areas of testing research, classified into two categories. Emerging areas are identified as new and challenging areas where innovative solutions are needed. Mature areas are identified as areas that have received extensive attention in the testing literature. In both categories, we identify areas of particular importance by pointing out that research in these areas is encouraged. Our classification of the various topics is based on the view that the goals of academic research are: (1) to provide algorithmic and methodological solutions, as opposed to production-ready tools, (2) to push the frontiers of knowledge, and (3) to produce results that impact industry practices. If these goals are met, high-quality training of graduate students will follow as a by-product.

In addition to discussing specific topics, we also call attention to certain of their characteristics, or attributes. When present, they may cause a sub-area to be classified as emerging or mature. We find that research involving circuits described at the RTL or higher levels of abstractions is emerging, whereas research on gate level circuits, combinational or sequential, is mature. Sequential circuit research is encouraged due to the fact that complete solutions are not available, and because of its applicability to other disciplines, such as verification. Other attributes of emerging areas include non-classical fault models, high-performance circuits, timing and delay issues, and core-based designs. Research for techniques to manage complexity, such as partitioning, test reuse, hierarchy, parallel processing is also encouraged.

Emerging Areas

In the following, we list the areas identified as emerging, divided into seven main topics.

1. Failure mechanisms and fault modeling.

This topic includes:

- Deep submicron defect issues:
  Many new defect types will exist in high density, high speed designs, including but not limited to: inductive/capacitive coupling, bridging, missing/extra vias, ground bounce, noise induced delay, process variations (which induces statistical departures from normal behavior that are indistinguishable from defects).
• Classification/detection/repair of manufacturing defects and performance problems in embedded arrays including DRAM, SRAM, CAM.
• Methods to identify/extract these defect types (e.g. from layout), then abstract them into tractable fault models, to generate patterns for them, compute and compare their coverages, to correlate these coverages to quality and yield metrics.
• Methods to correlate between high-level fault models (at the RTL and above) and low level fault models.

2. Debug, diagnosis, verification and failure analysis.

It includes:
• Diagnosis of failures due to defects discussed in Subsection 1 above.
• Fault diagnosis with BIST and design for BIST diagnosability.
• Diagnosis of reconfigurable architectures with FPGAs.
• Diagnosis of memories with redundancies.
• Design verification.

3. Performance testing

• High speed/frequency test.
  On-chip clock rates are expected to reach 2GHz by 2003. Testing in such chips will require, among other things, attention to energy consumption during switching, avoidance of added multiplexers in logic paths and careful consideration during ATPG of race conditions, multi-cycle delay paths, etc.
• Applying signals on chip with greater accuracy than available at the tester.
  Tester OTA is expected to stay about 200ps for the foreseeable future, resulting in the need to study how, e.g., 500ps waveforms can be measured with such accuracy.
• Delay test in multi-clock designs (synchronized or not), including on-chip generated clocks
• Delay testing incorporating interconnect, including both coupling capacitance and supply line effects and resistive bridges for many (e.g. 9) levels of metal.

4. Design methodologies.

The vast majority of design work now takes place at the RTL level and above, using behavioral and/or logic synthesis as integral part of design. DFT and BIST methods must continue to move to these levels in order to be effectively coupled with the design process. Similarly, chip design is increasingly making use of a systems approach, including reuse of embedded cores. Test methods that work with RTL and synthesis, and those which can be made to handle heterogeneous cores (asynchronous, mixed-signal, etc.) are encouraged. In the following, the emerging topics related to design methodologies are divided into four categories: Design for testability, Built-in-self-test, Synthesis for testability and On-line testing.

4. A Design for Testability

At the RTL and above.
  For systems-on-a-chip and embedded cores.
  For high-performance circuits.
  For circuits with primitives other than gates, such as tri-state elements
For asynchronous circuits
For analog and mixed signal circuits

4. B Built-In Self-Test
   For systems-on-a-chip and embedded cores
   For sequential circuits
   At-speed BIST
   For high-performance circuits

4.C Synthesis for testability
   Redundancy identification and removal for sequential circuits
   Identification of false paths in combinational and sequential circuits
   Circuit transformations to enhance testability

4.D. On-line testing
   System-level on-line testing

5. Test pattern generation.
   Test pattern generation must also follow the design trends discussed above. Test pattern generation procedures at the RTL and above will allow test pattern generation to be carried out in conjunction with design and design-for-testability efforts. Test pattern generation procedures need to accommodate the widespread use of reusable embedded cores. In addition, test pattern generation needs to address high performance circuits, and circuits with heterogeneous components. Specifically, the following topics were identified as emerging.
   At the RTL and above
   For high-performance circuits
   For circuits with primitives other than gates, such as tri-state elements
   For analog and mixed-signal circuits
   For asynchronous circuits
   For dynamic logic

6. ATE and measurement issues
   There is a great need for innovative research in wafer probing methods. As the number of pads on a die increases, with the increasing importance of shipping known good die, as the pad placement changes from edge to area array, and as the speed of signals needed to cross the chip boundary increases, the current techniques are reaching their limitations. In addition to extensions of current techniques, studies in contactless probing; e.g. optical testing methods, are encouraged.
   There is a need to reduce, across the board, the amount of information that must be exchanged between the device and the tester, and lower the frequency at which that information is exchanged. This is because the volume of data needed to test a gate is remaining relatively constant while the number of gates increases by 30% per year and the communication bandwidth between the tester and the chip is not keeping up.
   As conventional single-threshold IDDQ testing loses steam in deep submicron processes, new techniques which offer similar capabilities are needed. Examples of these IDDQ extensions/replacement methods include current signatures, very low voltage tests, and dynamic current or
power supply voltage methods. There are also opportunities to develop other parametric test methods, such as optical, EM field, temperature, etc.

7. Analog and mixed signal testing including MEMS and sensor technologies
   - Correlation between system failures and physical causes such as process variations and defects.
   - Modeling of faults at higher levels of abstraction, e.g., behavioral fault modeling and fault macromodeling.
   - On-chip parametric measurement, leading to possible Pass/Fail decisions.
   - Quality metrics (e.g. figure of merit) for mixed-signal test: when is a chip good enough to be sent to a customer?
   - Mixed-signal DFT/BIST, especially at higher frequencies.
   - High-frequency measurement techniques, especially using statistical models to extract parameters via indirect measurements.
   - Verification techniques during the design process.
   - Test program generation, fault simulation and validation tools.
   - Signal acquisition and delivery under effects of hardware and parasitics,
   - Test set design to reduce test time and cost of test hardware.

Mature Areas

In the following, we list the areas identified as mature, divided into five main topics. It is important to stress that novel solutions to any problem are always welcome.

1. Design methodologies

1.A DFT
   - Synthesis of scan chains, and integration of scan functionality into design
   - Partial scan selection techniques at the gate level
   - Test-point insertion at the gate level

1.B BIST
   - Synthesis for random pattern testability
   - Built-in test pattern generators for combinational and full-scan circuits
   - Response compactors and aliasing probability
   - Memory BIST
   - Modifications to test pattern generators to add deterministic patterns.

1.C Synthesis for testability
   - Redundancy identification in combinational circuits

1.D. On-line testing
   - Self-checking circuits

2. IDDQ testing
   - Single pass/fail threshold IDDQ testing
Built-in current sensors (BICSs)

3. Test pattern generation and fault simulation
   For combinational circuits
   For sequential circuits. However, research on sequential ATPG is encouraged.
   Memory test based on functional fault models
   Combinational vector compaction

4. Debug, diagnosis and failure analysis
   Diagnosis which uses a single fault assumption from any of the "classical" models (stuck-at, wired-logic bridging, stuck-open, stuck-on)

5. Other topics
   Test economics
   PLA testing
   Functional testing of standalone A/D, D/A, op amp and RC circuits without measurement limitations